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IH81M

Version : 0E

CPU :

Intel Haswell Processor

System Chipset :

Intel Lynx Point Chipset

On Board Chipset :

VRM 12.5 -- NCP81102+NCP81161 4Phase

Gigabit LAN -- RTL8111GN Co-lay RTL8111E-VC

HDA Codec -- Realtek ALC662VD

Super I/O -- NCT6779D

SPI Flash 64Mb

Main Memory :

2 Channel DDR III * 2 (Max 16GB)

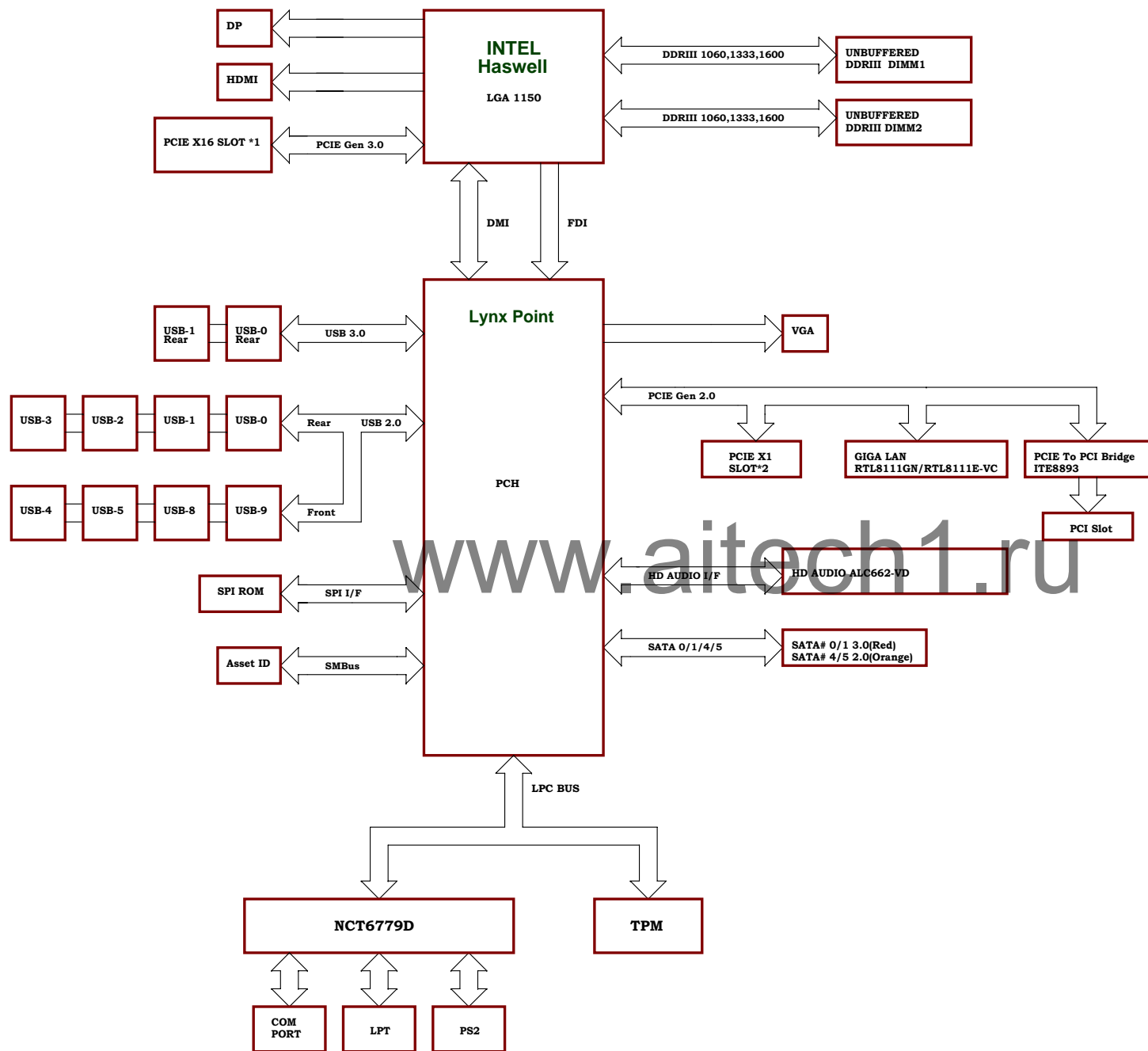
Expansion Slot :

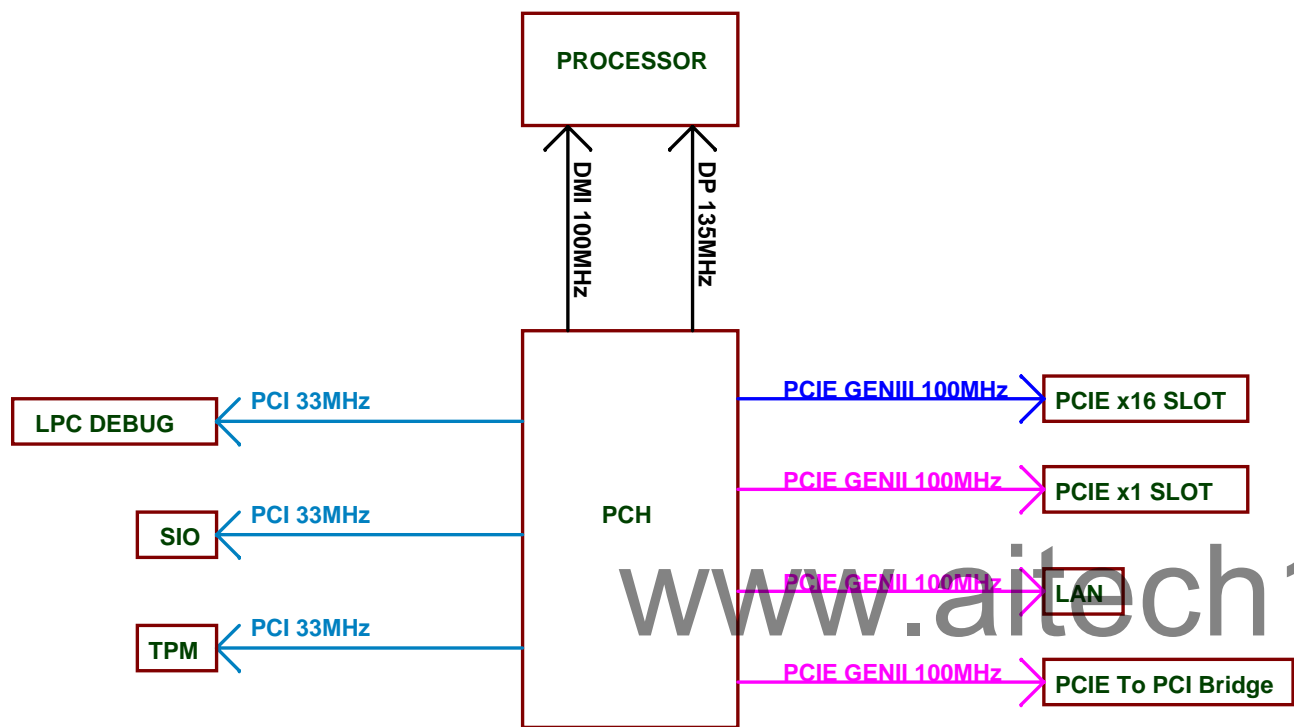
PCI Express x16 Slot * 1

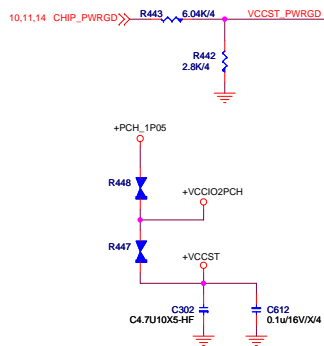
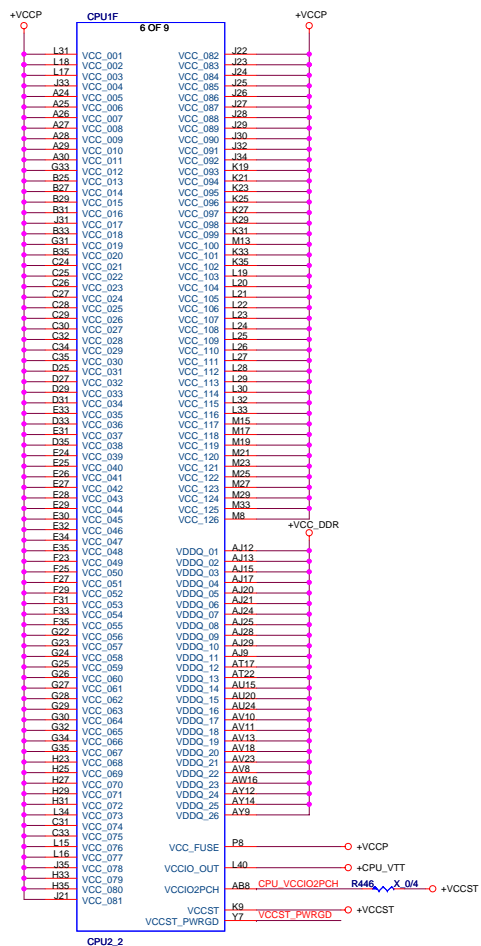
PCI Express x1 Slot * 2

PCI Slot * 1

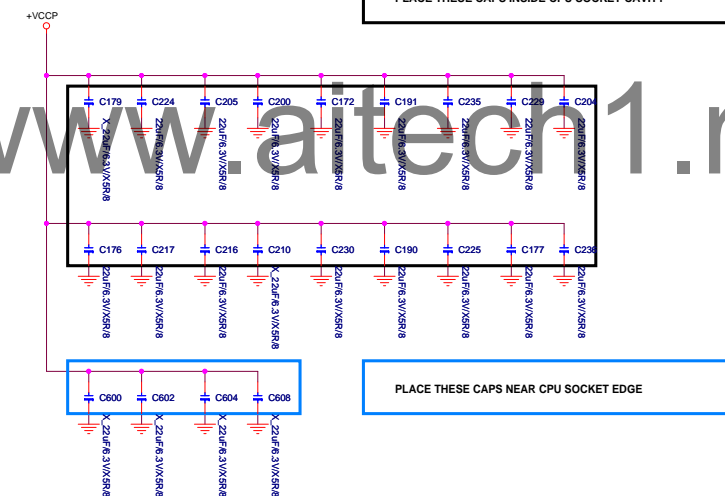




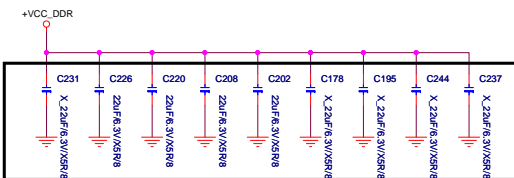


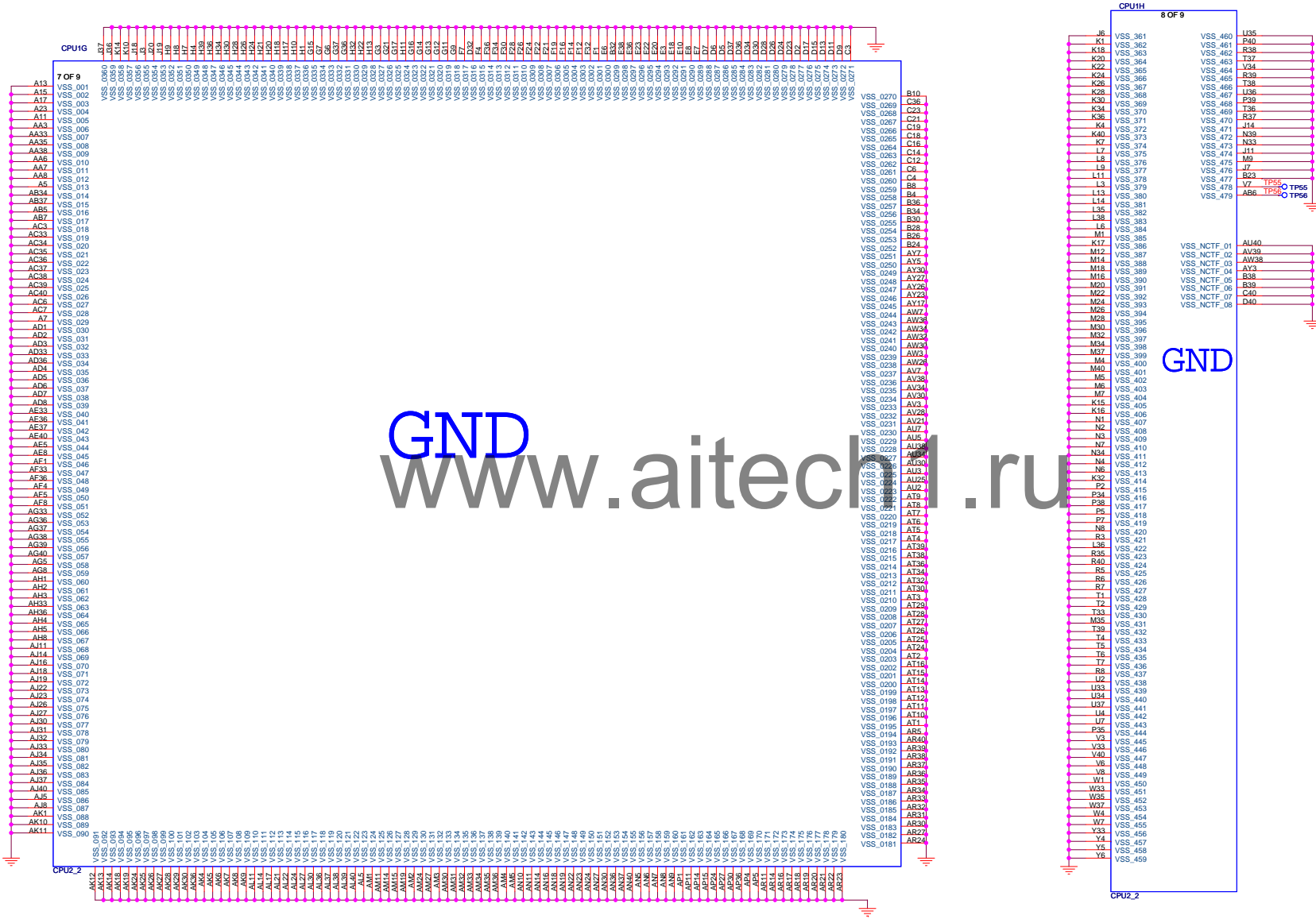


VCCP-Decoupling



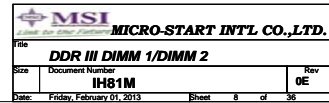
VCC_DDR-Decoupling





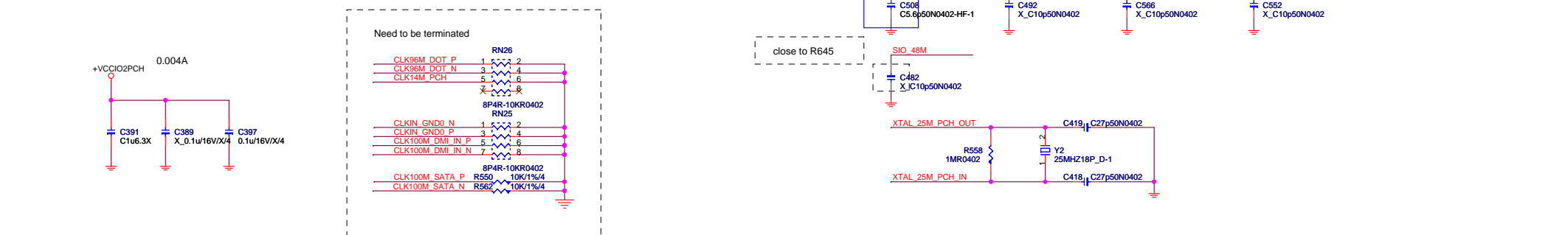
Palce Caps Between CHA And CHB

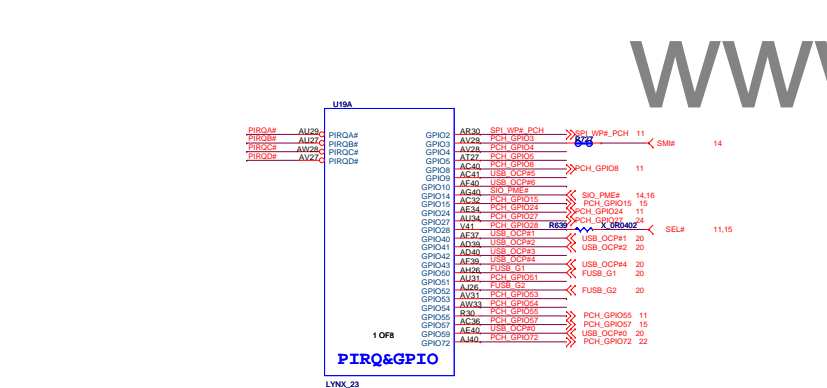
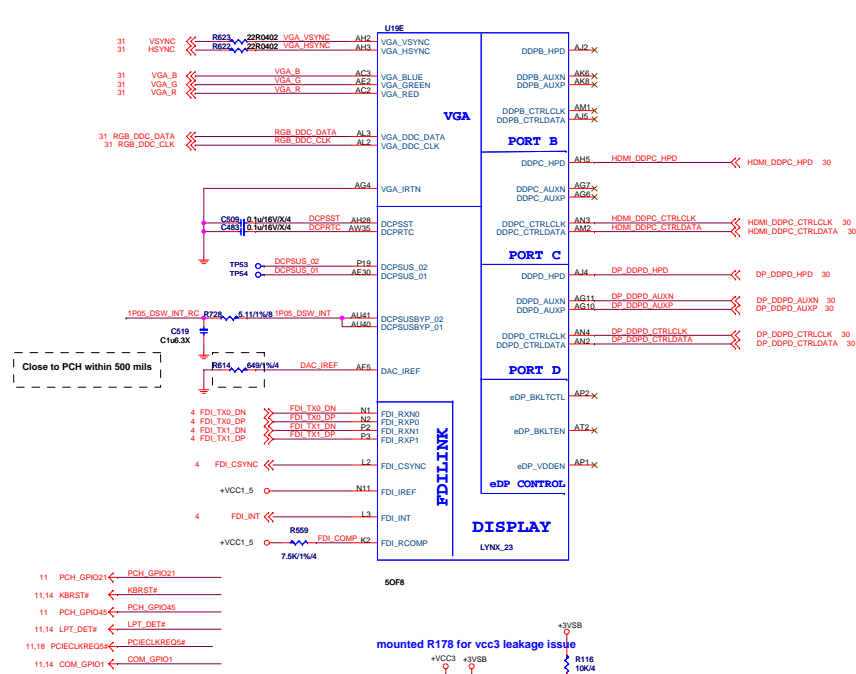
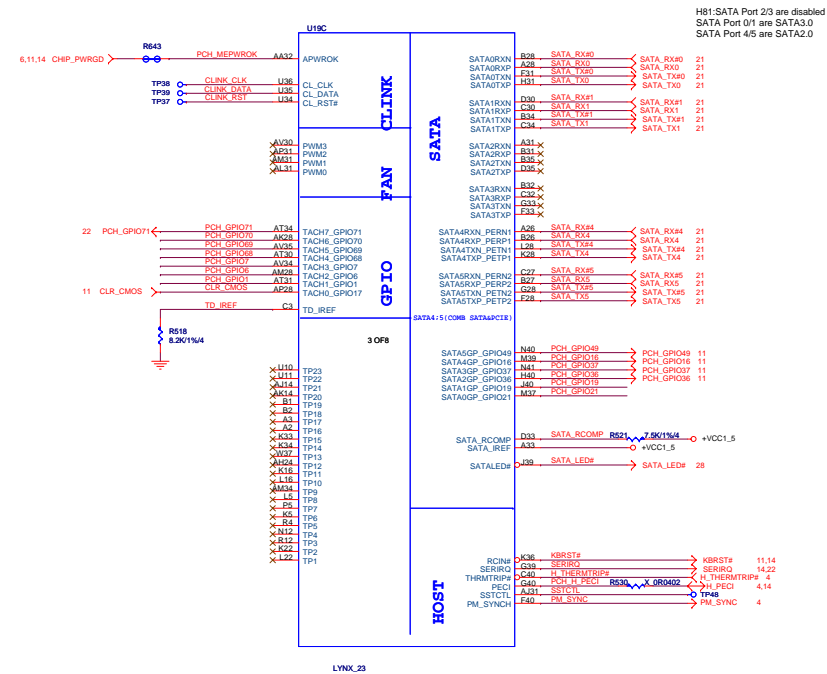






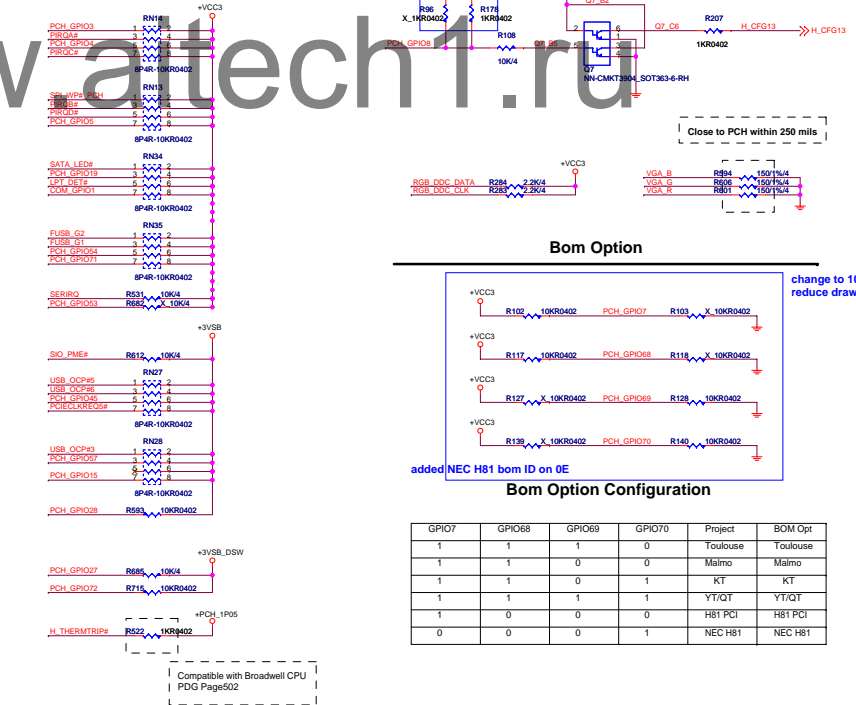
LYNX_23 2 OF 8



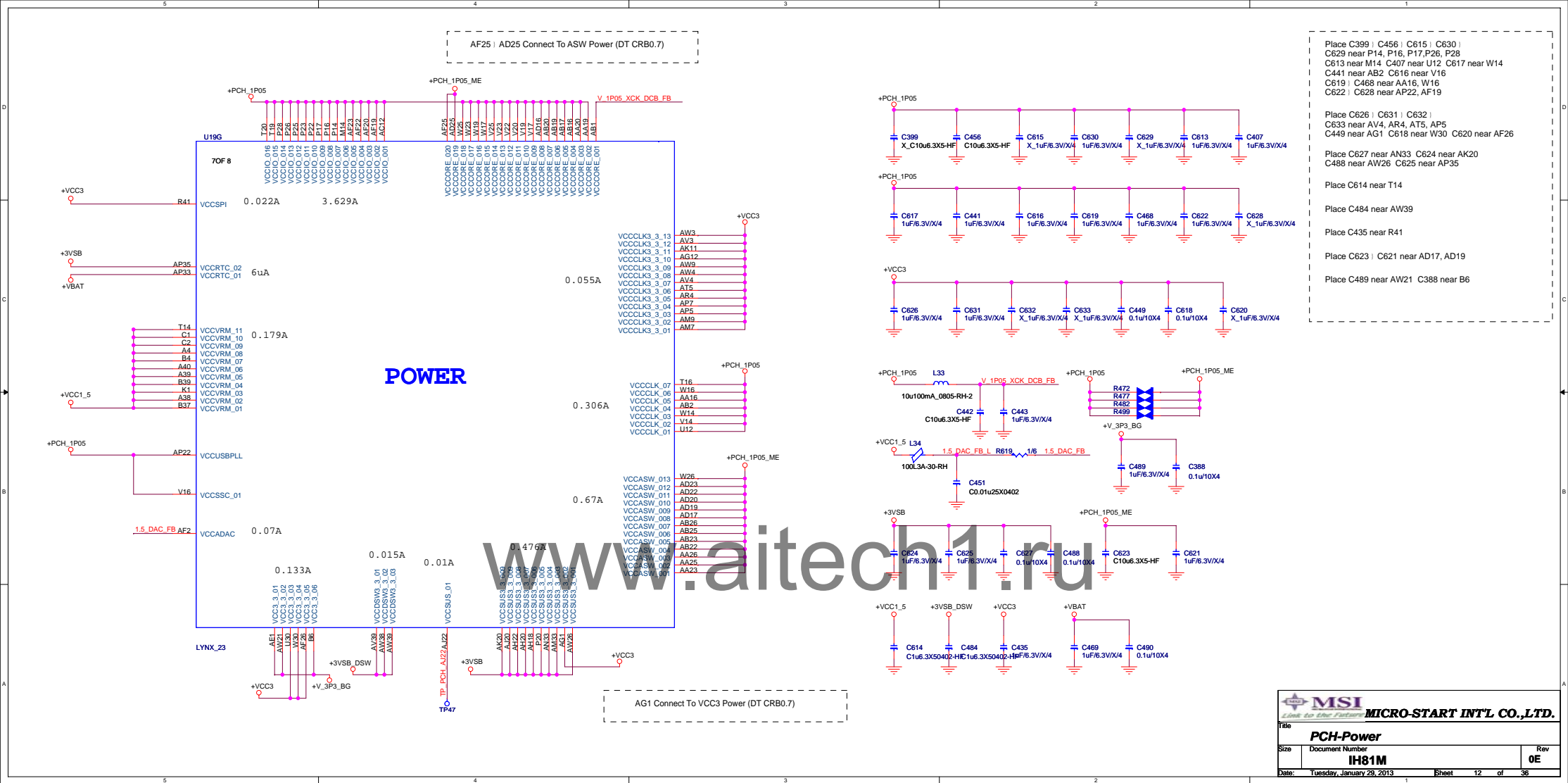


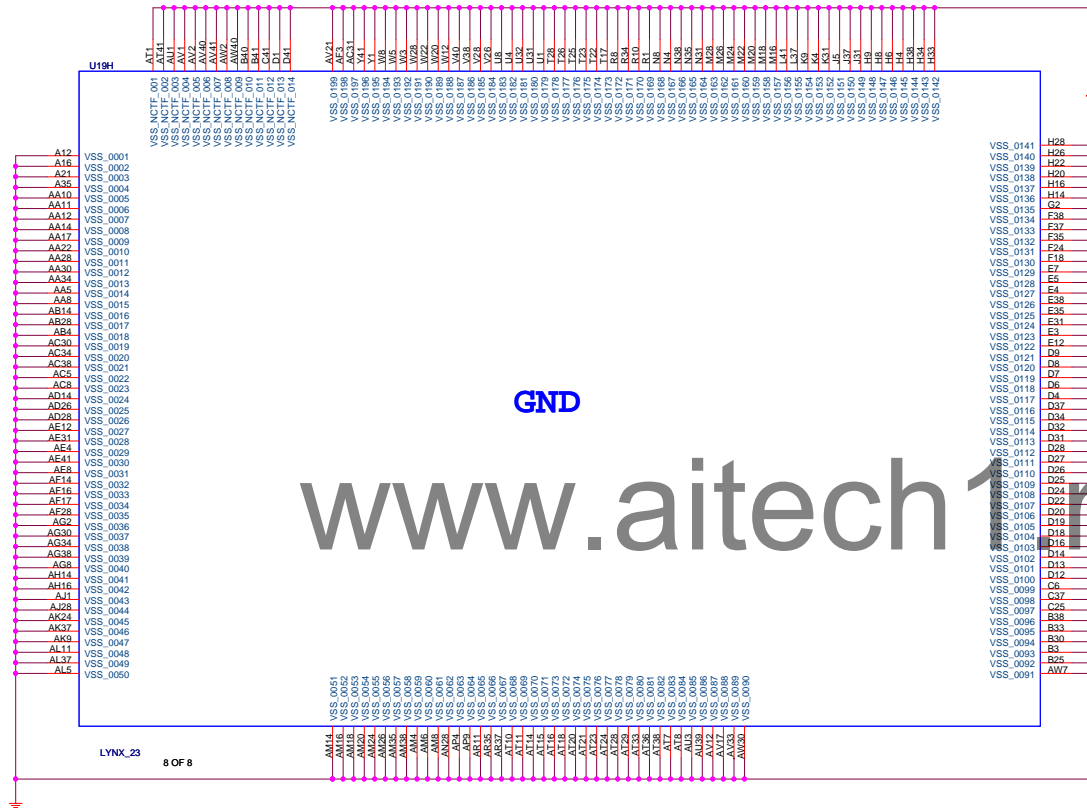
| BIOS STARAPS | | |
|--------------|-------|-------|
| BIOS STARAPS | GPIO1 | GPIO6 |
| 0A | 1 | 1 |
| NA | 0 | 0 |

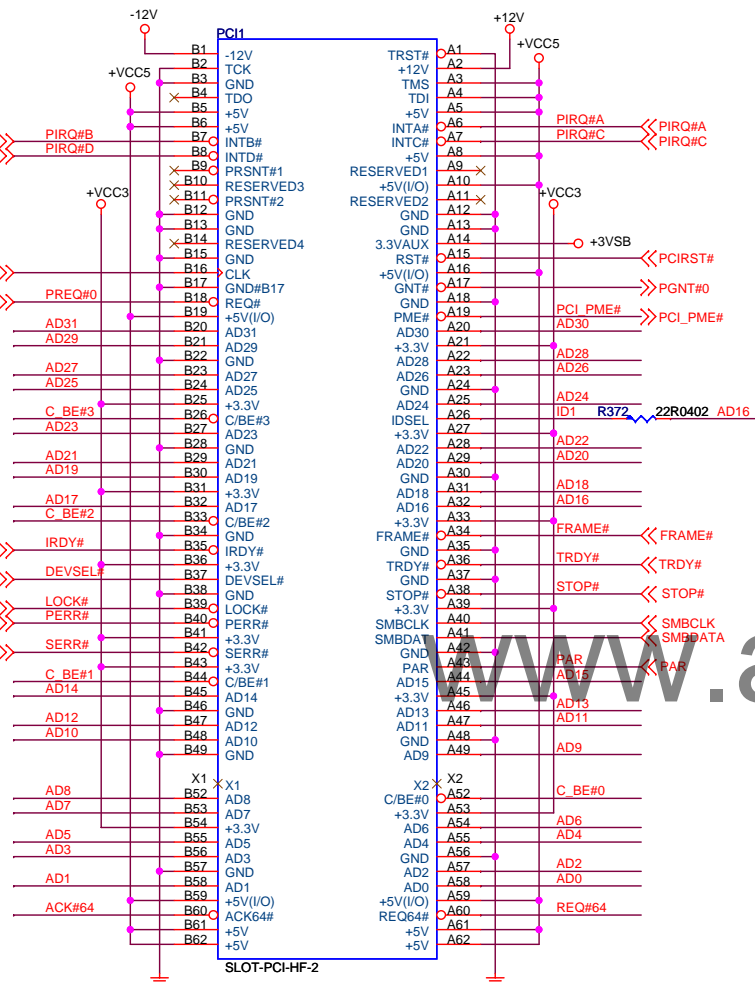
| BIOS Device Select | | |
|--------------------|--------|--------|
| BOOT DEVICE | GPIO51 | GPIO19 |
| LPC | 0 | 0 |
| SPI | 1 | 1 |



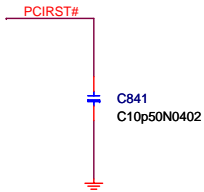
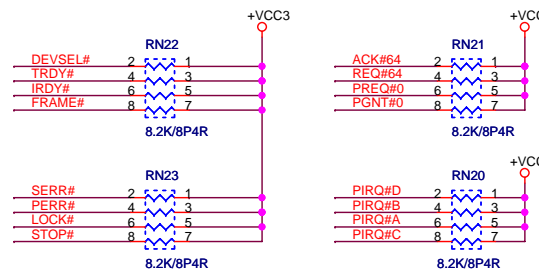
| GPIO7 | GPIO68 | GPIO69 | GPIO70 | Project | BOM Opt |
|-------|--------|--------|--------|----------|----------|
| 1 | 1 | 1 | 0 | Toulouse | Toulouse |
| 1 | 1 | 0 | 0 | Malmö | Malmö |
| 1 | 1 | 0 | 1 | KT | KT |
| 1 | 1 | 1 | 1 | YT/QT | YT/QT |
| 1 | 0 | 0 | 0 | H81 PCI | H81 PCI |
| 0 | 0 | 0 | 1 | NEC H81 | NEC H81 |





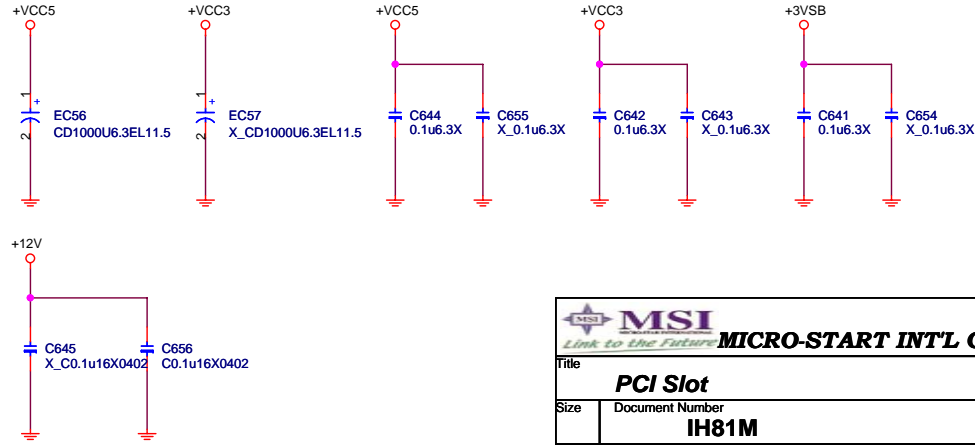


PCI PULL-UP / DOWN RESISTORS



PCI slot

| | | |
|-------|-----------|---------|
| +3VSB | (wake) | - 375mA |
| +3VSB | (no wake) | - 20mA |
| +3.3V | | - 7.6A |
| +5V | | 5A |
| +12V | | 0.5A |



MSI
Link to the Future

MICRO-START INTL CO.,LTD.

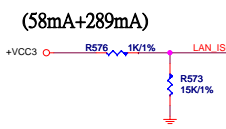
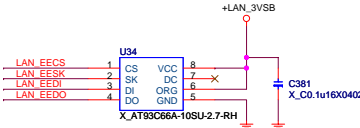
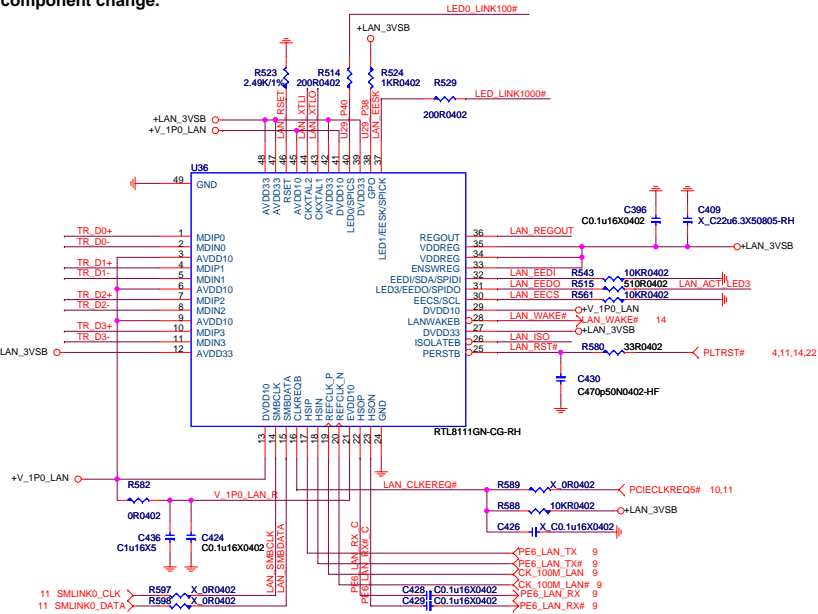
Title: **PCI Slot**

Size: Document Number **IH81M** Rev **0E**

Date: Friday, January 11, 2013 Sheet 17 of 36

Gigabit LAN RTL8111E-VC Co-lay RTL8111GN

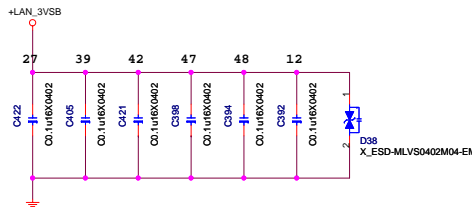
RTL8111E-VC is pin to pin compatible with RTL8111GN.
The two chips can change each other without any component change.



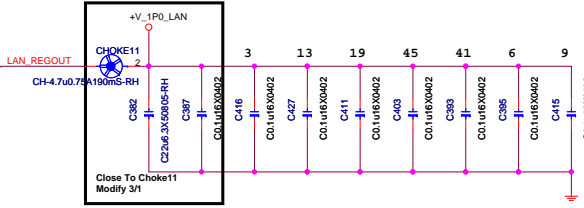
| WOL | status | Yellow | Gm/Org |
|-----|---------------|--------|--------|
| off | No Link | off | off |
| on | S3/S4/S5 | off | off |
| on | 10M.inactive | off | off |
| on | 10M.active | off | off |
| on | 100M.inactive | off | off |
| on | 100M.active | off | off |
| on | 1G.inactive | off | off |
| on | 1G.active | off | off |

always on
always on
always on
blinking

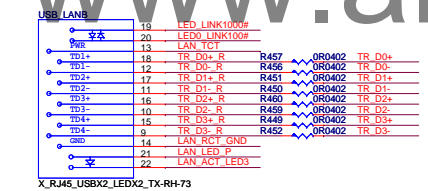
Place Near Pin



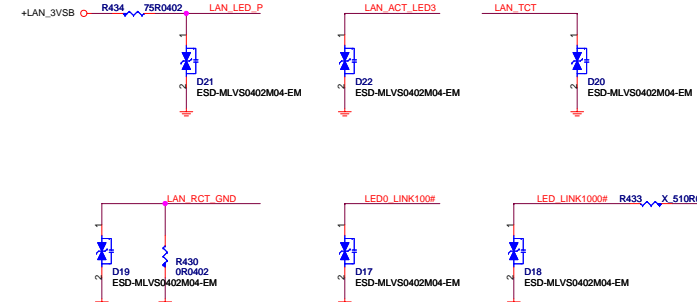
Place Near Pin



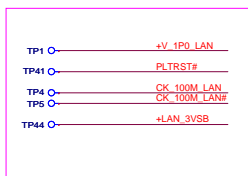
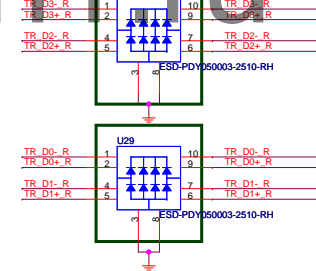
LAN Connector



ESD

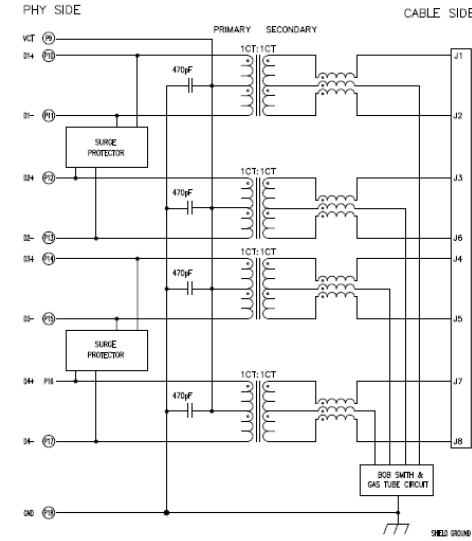


ESD



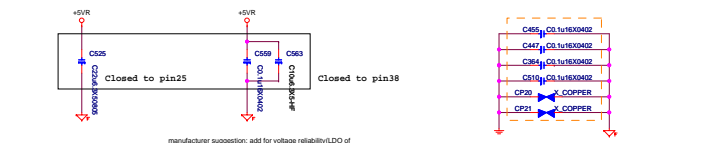
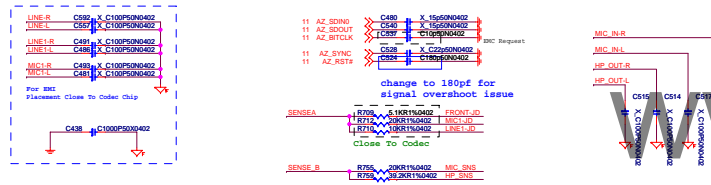
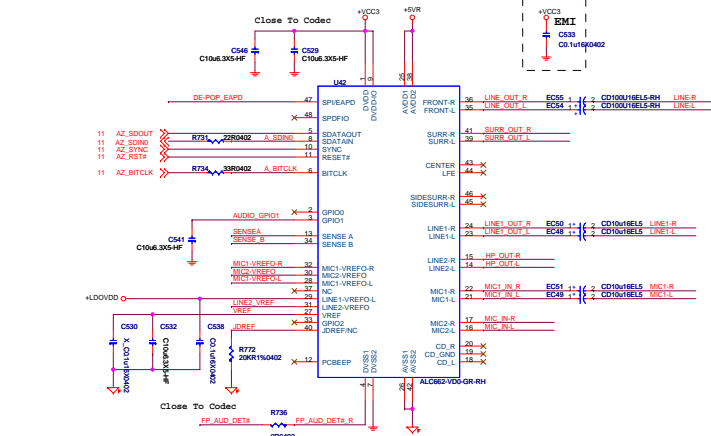
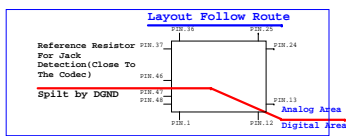
EMI solution: can be unmounted if LAN connector has surge protect

SCHEMATIC



Azalia Codec - ALC662-VD

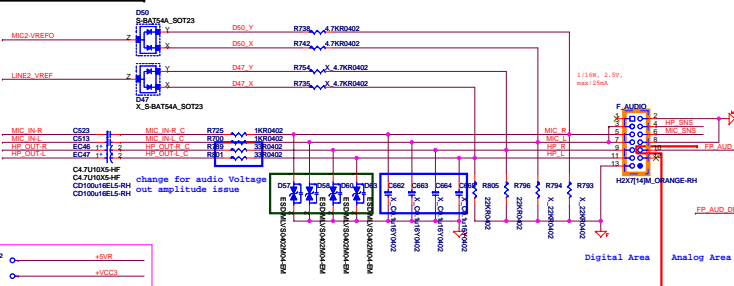
removed ALC662VC co-layer schematic on OD



manufacturer suggestion: add for voltage reliability(LDO of audio chip shales with reason what we don't know)

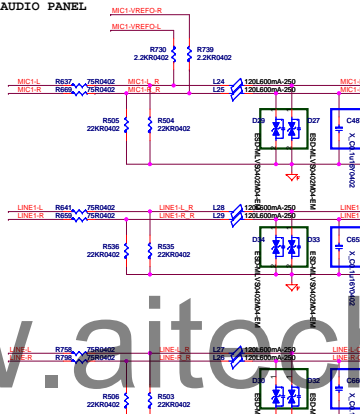
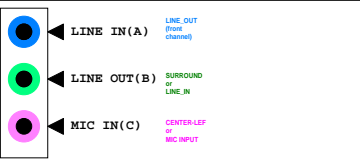
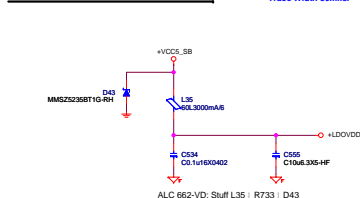
EMC Request

Front Audio Jack

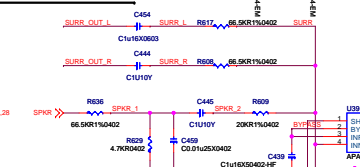


AUDIO CODE REGULATORS

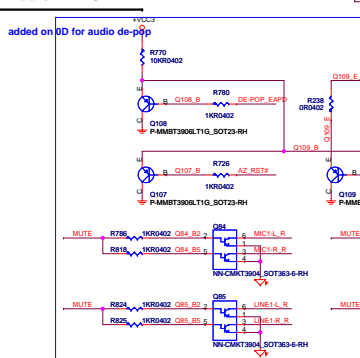
Trace Width 30mils.



MONO Amplifier



Audio DE-POP



The top diagram illustrates the USB to RS-485 interface. It features a MAX3232CPE (U1) for USB to UART conversion and a MAX485 (U2) for RS-485 conversion. The USB side includes a USB_EN# pin connected to a 10k resistor (R800) and a USB_S# pin connected to a 0R0402 resistor. The UART side includes a TX pin connected to a 10k resistor (R782) and a RX pin connected to a 10k resistor (R782). The RS-485 side includes an A pin connected to a 10k resistor (R782) and a B pin connected to a 10k resistor (R782). The power supply is +VCC5_S8, and the ground is GND.

The bottom diagram illustrates the RS-485 to RS-485 interface. It features two MAX485 (U1 and U2) for RS-485 conversion. The RS-485 side includes an A pin connected to a 10k resistor (R772) and a B pin connected to a 10k resistor (R772). The power supply is +VCC5_S8, and the ground is GND.

[illegible]

The top diagram illustrates the USB to UART conversion circuit. It features a CP2102N IC (labeled U27) which interfaces between a USB port and a microcontroller's UART pins. The USB signals (USB_#) are connected to the IC's pins, and the IC's UART pins are connected to the microcontroller's UART pins. The circuit also includes a +VCC5_SB supply and a C285 capacitor.

The bottom diagram illustrates the RS-485 driver circuit. It features a CML4-12-9008100-HF IC (labeled U4) which drives the RS-485 signals. The microcontroller's RS-485 pins are connected to the IC's pins, and the IC's pins are connected to the RS-485 network. The circuit also includes a +VCC5_SB supply and a C285 capacitor.

The schematic diagram illustrates the USB-to-serial interface circuit. It includes a USB-to-serial converter IC, the NP-P90030VGS_SOIC8-RH, which is connected to a USB port (C170, C0.1uF16X0402) and a serial port (C142, C0.1uF16X0402). The USB port is connected to +VCC5 and +VCC5B. The serial port is connected to +VCC5B and +VCC5. The IC has pins 1, 2, 3, 4, 5, 6, 7, and 8. Pin 1 is connected to +VCC5B. Pin 2 is connected to +VCC5. Pin 3 is connected to +VCC5B. Pin 4 is connected to +VCC5. Pin 5 is connected to +VCC5B. Pin 6 is connected to +VCC5. Pin 7 is connected to +VCC5B. Pin 8 is connected to +VCC5. The IC is also connected to a USB port (C170, C0.1uF16X0402) and a serial port (C142, C0.1uF16X0402). The USB port is connected to +VCC5 and +VCC5B. The serial port is connected to +VCC5B and +VCC5. The IC has pins 1, 2, 3, 4, 5, 6, 7, and 8. Pin 1 is connected to +VCC5B. Pin 2 is connected to +VCC5. Pin 3 is connected to +VCC5B. Pin 4 is connected to +VCC5. Pin 5 is connected to +VCC5B. Pin 6 is connected to +VCC5. Pin 7 is connected to +VCC5B. Pin 8 is connected to +VCC5.

+RUSB9_SVCC1 R55 10KR15M0402 USB_OCP#0
 R54 15KR15M0402
 +RUSB3_SVCC2 R316 10KR15M0402 USB_OCP#0
 R323 15KR15M0402
 +5VUSB_SVCC3 R792 10KR15M0402 USB_OCP#2
 R798 15KR15M0402
 +5VUSB_SVCC2 R787 10KR15M0402 USB_OCP#1
 R802 15KR15M0402
 +5VUSB_SVCC1 R68 10KR15M0402 USB_OCP#4
 R67 15KR15M0402

The schematic diagram illustrates the USB3.0 differential signal traces. It shows four pairs of differential signal traces, each pair consisting of a driver and a receiver connected to a common mode choke (CMC-L12-9000) and a 100pF capacitor. The traces are labeled with USB3 TX0, TX1, RX0, RX1 and their differential counterparts (DN, DP, R).

- TX0 Pair:** Driver L12 (R329, R336, X GR0402) and Receiver R329 (R336, X GR0402) connected to CMC-L12-9000 and 100pF. Traces: USB3 TX0, C DN, R; USB3 TX0, C DP, R.
- TX1 Pair:** Driver L10 (R336, R336, X GR0402) and Receiver R336 (R336, X GR0402) connected to CMC-L12-9000 and 100pF. Traces: USB3 TX1, C DN, R; USB3 TX1, C DP, R.
- RX0 Pair:** Driver L18 (R360, R360, X GR0402) and Receiver R360 (R360, X GR0402) connected to CMC-L12-9000 and 100pF. Traces: USB3 RX0, DN, R; USB3 RX0, DP, R.
- RX1 Pair:** Driver L16 (R378, R378, X GR0402) and Receiver R378 (R378, X GR0402) connected to CMC-L12-9000 and 100pF. Traces: USB3 RX1, DN, R; USB3 RX1, DP, R.

SATA7PM_RED-ST-RH+1

| Signal | Pin | Connector Pin |
|-----------|------|---------------------|
| SATA_RX0 | C466 | 0.01u16X0402 S_RX0 |
| SATA_RX0# | C465 | 0.01u16X0402 S_RX0# |
| SATA_TX0 | C464 | 0.01u16X0402 S_TX0 |
| SATA_TX0# | C463 | 0.01u16X0402 S_TX0# |

SATA7PM_ORANGE-P-RH

| Signal | Pin | Connector Pin |
|-----------|------|---------------------|
| SATA_RX4 | C500 | 0.01u16X0402 S_RX4 |
| SATA_RX4# | C499 | 0.01u16X0402 S_RX4# |
| SATA_TX4 | C498 | 0.01u16X0402 S_TX4 |
| SATA_TX4# | C497 | 0.01u16X0402 S_TX4# |

SATA3

| Signal | Pin | Connector Pin |
|-----------|------|---------------------|
| SATA_RX1 | C474 | 0.01u16X0402 S_RX1 |
| SATA_RX1# | C473 | 0.01u16X0402 S_RX1# |
| SATA_TX1 | C471 | 0.01u16X0402 S_TX1 |
| SATA_TX1# | C470 | 0.01u16X0402 S_TX1# |

SATA4

| Signal | Pin | Connector Pin |
|-----------|------|---------------------|
| SATA_RX5 | C504 | 0.01u16X0402 S_RX5 |
| SATA_RX5# | C503 | 0.01u16X0402 S_RX5# |
| SATA_TX5 | C502 | 0.01u16X0402 S_TX5 |
| SATA_TX5# | C501 | 0.01u16X0402 S_TX5# |

change fan name to capital

The schematic diagram illustrates the electrical connections for the CPU-FAN module. Key components and connections include:

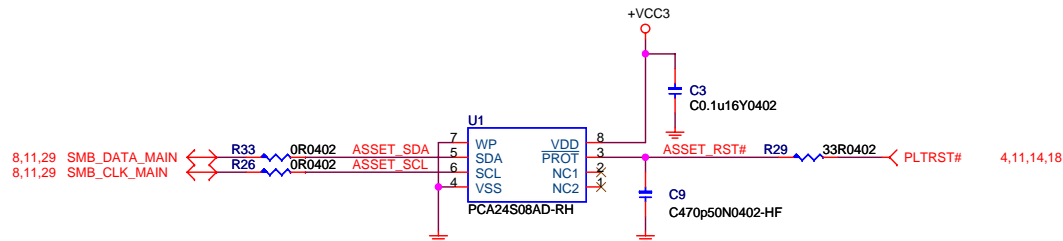
- Power Supply:** +12V and +VCC5 rails are shown. The +12V rail is connected to the CPU-FAN module via a diode (D1) and a resistor (R39). The +VCC5 rail is connected to the CPU-FAN module via a resistor (R163).
- Control Signals:** The CPU-FAN module has two control signals: CPU-FAN_CTL_G1 and CPU-FAN_CTL_G2. These signals are connected to the CPU-FAN module via resistors (R163 and R164).
- Temperature Sensor:** The CPU-FAN module includes a temperature sensor (BHTX48_BROWN-RH) connected to the CPU-FAN module via a resistor (R906).
- Grounding:** The CPU-FAN module is grounded to the system ground via a resistor (R41).
- Other Components:** The diagram also shows a capacitor (C23) connected to the +12V rail, a diode (D3) connected to the +VCC5 rail, and a MOSFET (Q10) connected to the CPU-FAN module.

change to 4 pin smart fan on 0D

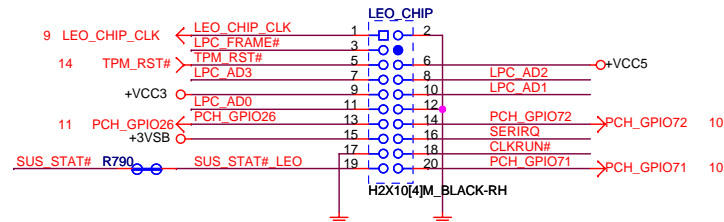
The schematic shows the AUX-FAN control circuit. It includes a +12V supply connected through D44C and BAS32L LL34 diodes to R547 (4.7K) and R545 (27K). A CD100U16EL capacitor is connected to ground. The circuit also features a +VCC5 supply connected through R556 (4.7K) and R580 (A7KR0402) to the G2 pin of C88 (NN-2N7002D MOSFET). The MOSFET's gate is also connected to the G1 pin of R567 (0R0402) and the D2 pin of R512 (A7KR0402). The MOSFET's drain is connected to the fan motor (represented by a circle with a triangle) and the DZ pin of R512. The MOSFET's source is connected to ground. The fan motor is labeled AUX2_FAN and has pins 1, 2, and 3. Pin 1 is connected to +12V, pin 2 is connected to ground, and pin 3 is connected to the G1 pin of R567. The fan motor is also connected to the DZ pin of R512. The fan motor is labeled AUX2_FAN and has pins 1, 2, and 3. Pin 1 is connected to +12V, pin 2 is connected to ground, and pin 3 is connected to the G1 pin of R567. The fan motor is also connected to the DZ pin of R512.

[illegible]

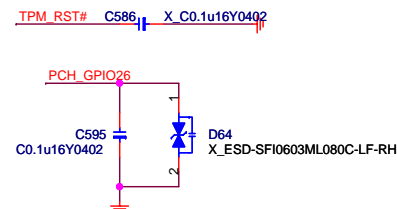
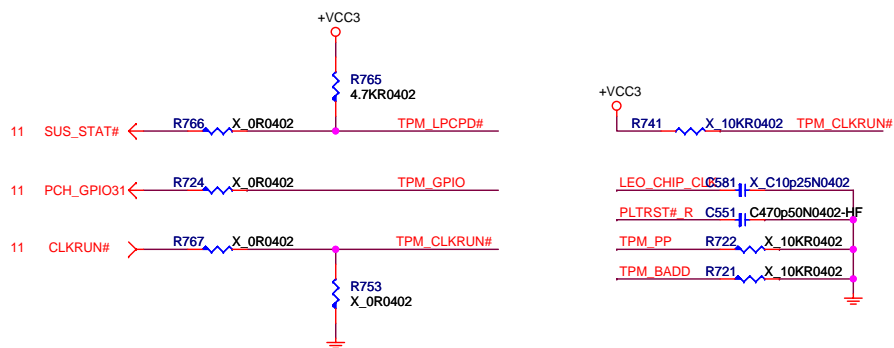
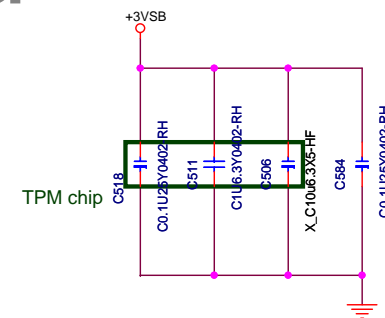
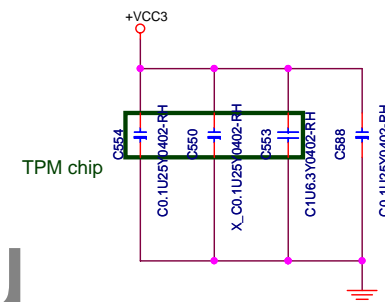
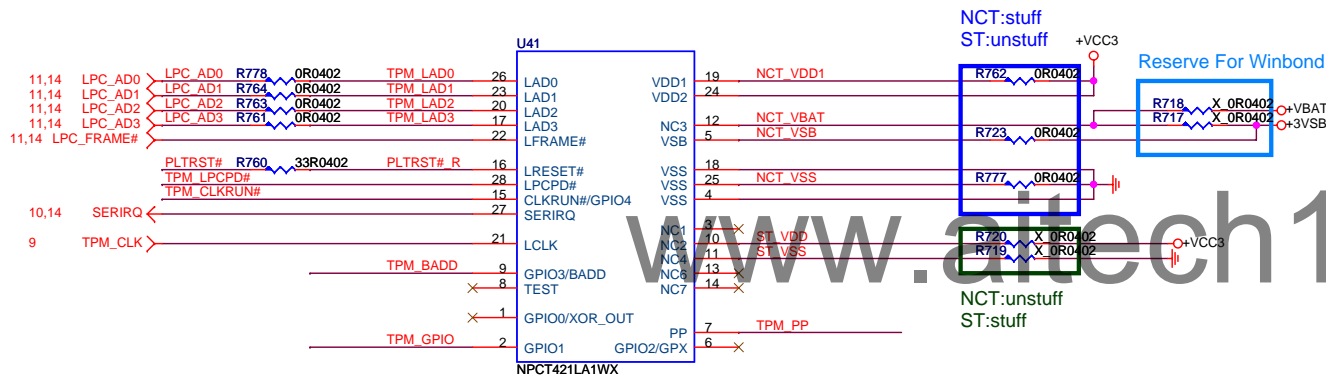
Asset ID



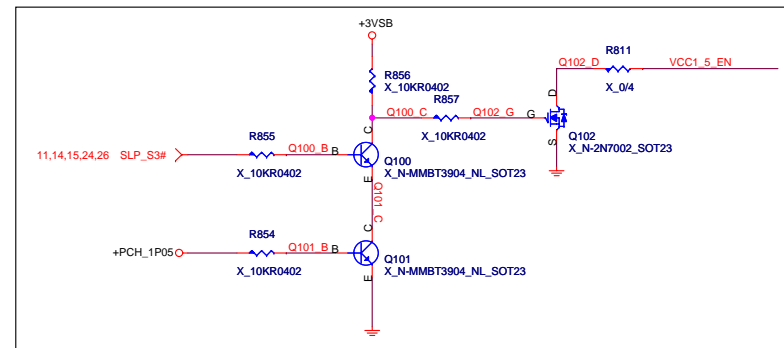
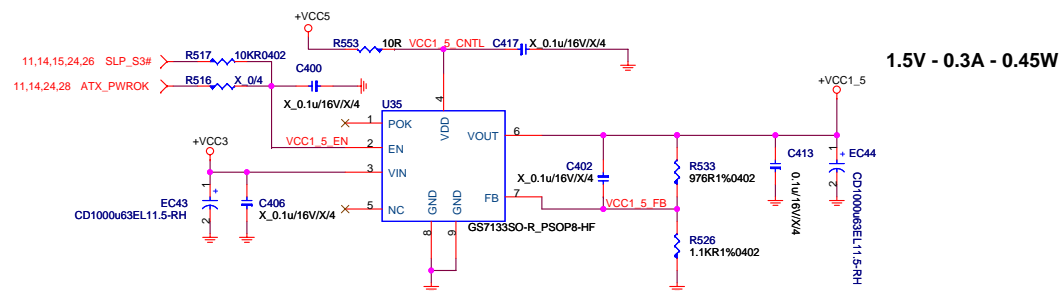
TCM Header



TPM



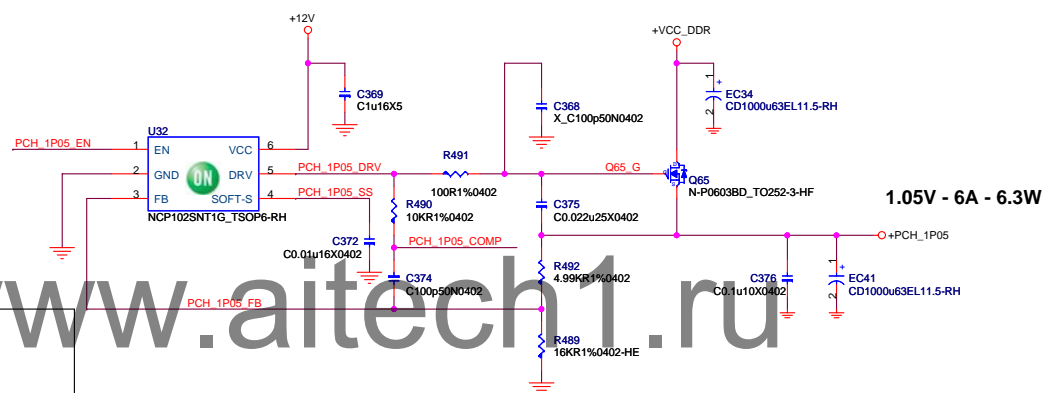
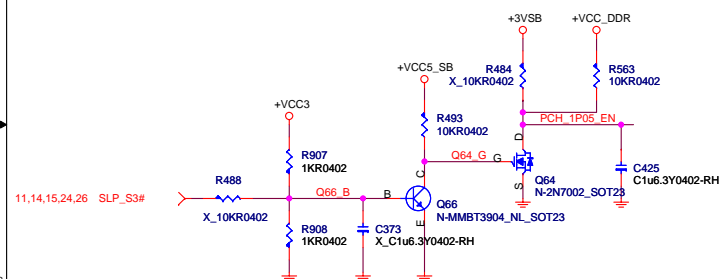
1.5V Power



sequence requirement on VCC1_5 and PCH_1P05

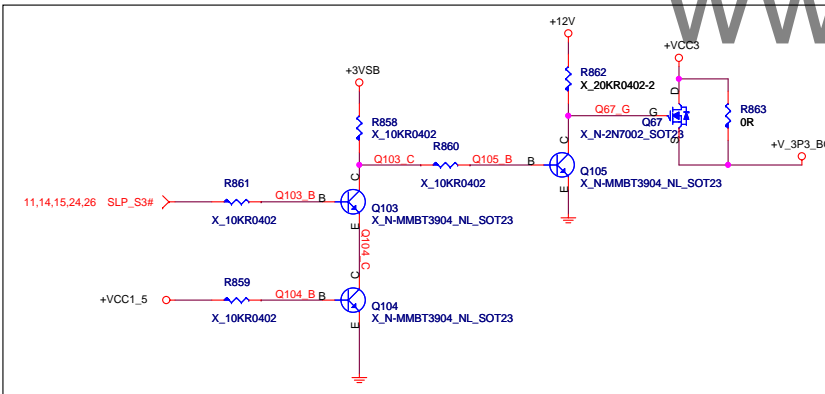
PCH Core Power Control


PCH Core Power

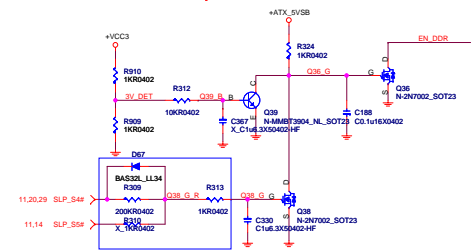


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VCC3_3 pins on the Core well (AE1, B6, AW21) have a sequencing requirement with respect to the PCH Core 1.05V rail (VCC)

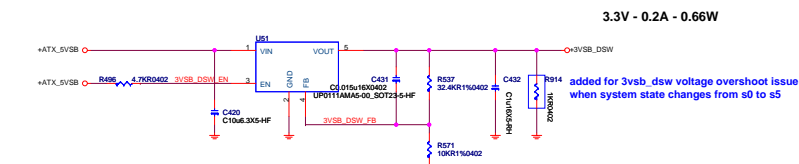


| | | |
|---|--------------------------|----------------|
|  MICRO-START INT'L CO.,LTD. | | |
| PCH & ME Core Power | | |
| Size | Document Number | Rev |
| | IH81M | 0E |
| Date: | Friday, January 11, 2013 | Sheet 23 of 36 |

$$V_{out} = 0.8[(R_{254} + R_{246}) / R_{254}]$$


change for lenovo request

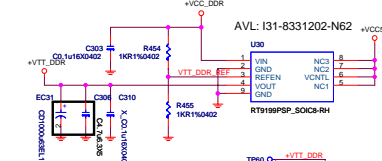
Deep Sx Power For Wake On Lan



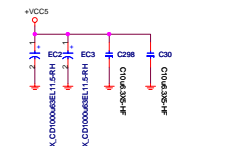
3.3V - 0.2A - 0.66W

⁴ added for 3vsb_dsw voltage overshoot issue when system state changes from s0 to s5

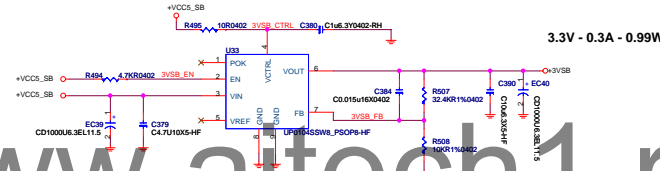
0.75V - 1.1A - 0.825W



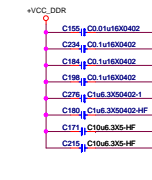
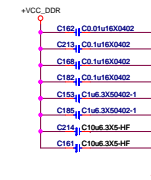
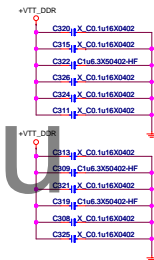
DDRIII I/O power decoupling caps.



AVL: I31-7133S02-N03/I31-3730S02-N62

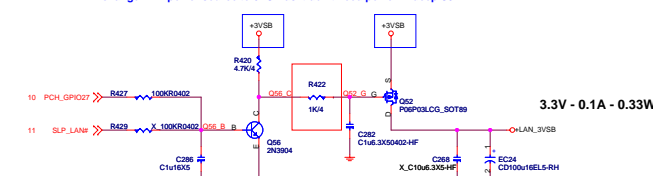


3.3V - 0.3A - 0.99W

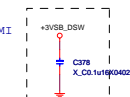
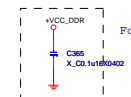
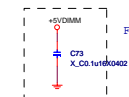


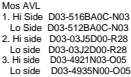
change LAN power source to 3VSB as it don't need power in deep S5

change LAN power source to 3VSB as it don't need power in deep S5



3.3V - 0.1A - 0.33W



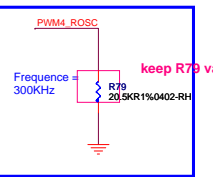
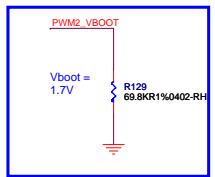
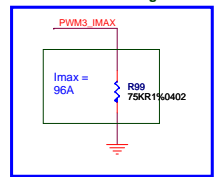
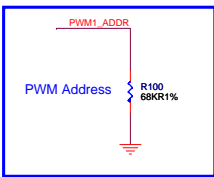
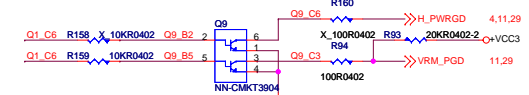
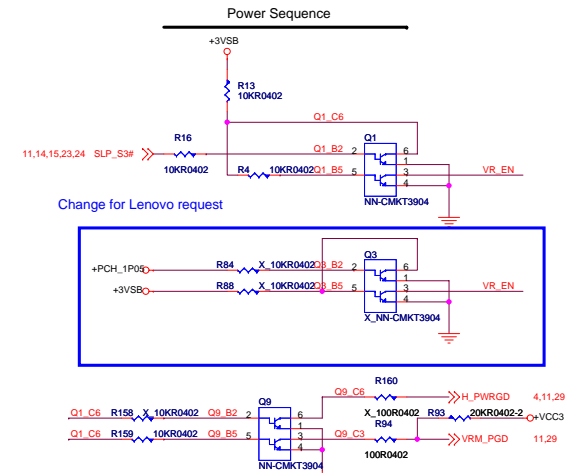
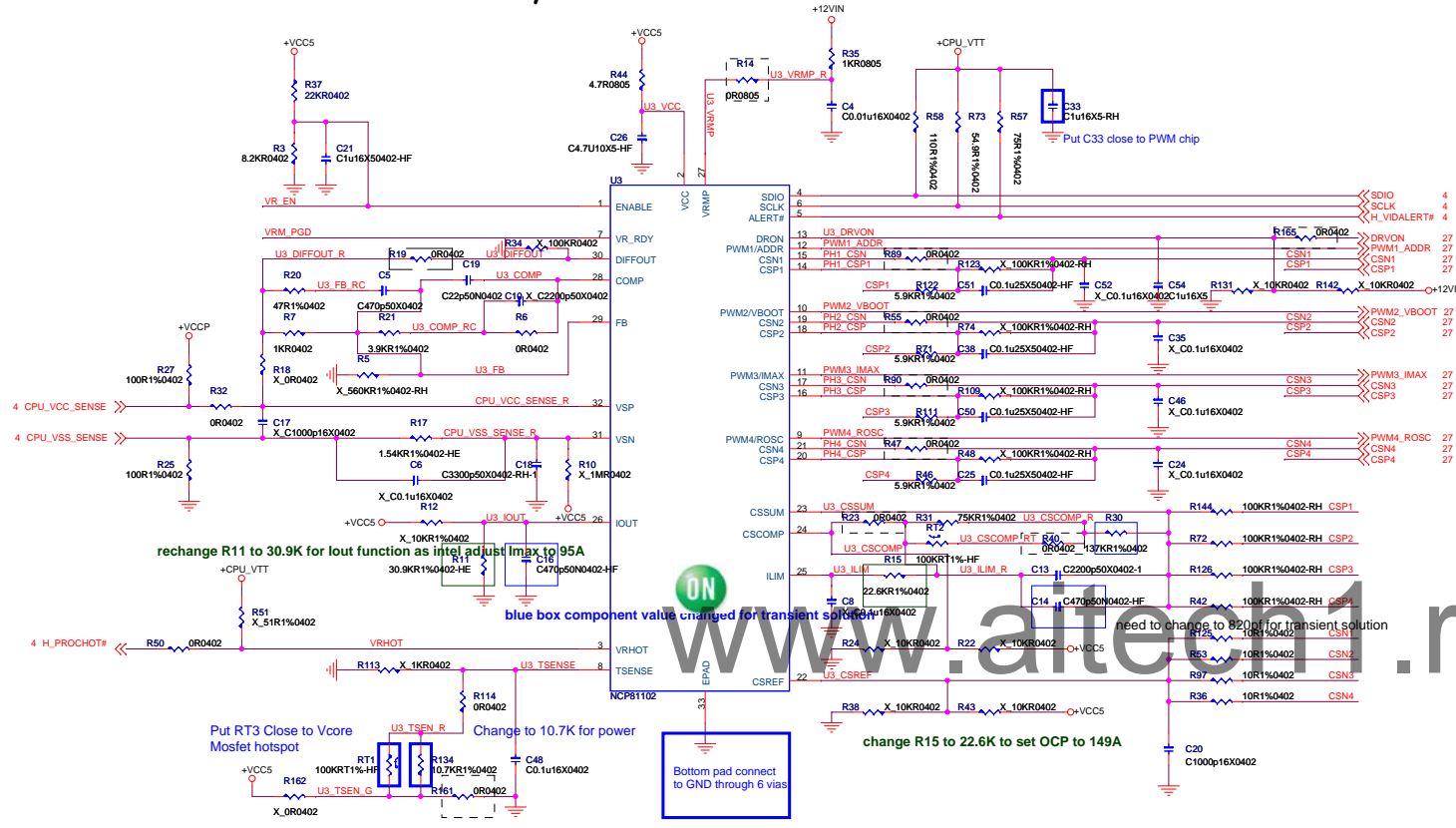


DCM programming pin:

- Ground this pin to setup automatic CCM-DCM transfer without minimum switching frequency limitation;
- Connect this pin to VCC to force CCM operation;
- Leave this pin open to give automatic CCM-DCM transfer, but with minimum switching frequency of 33KHz.



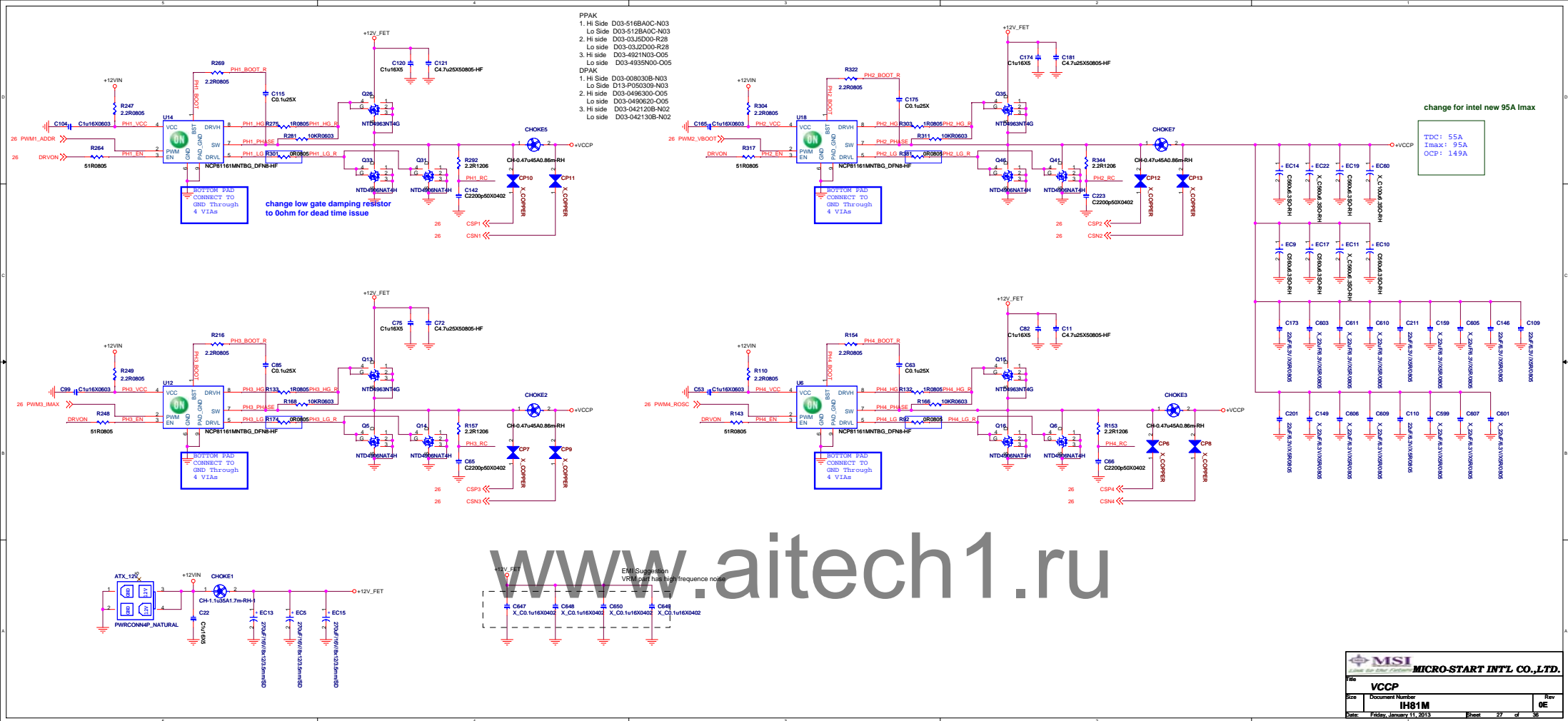
SharkBay VR12.5 Power Circuit - 4 Phase



| Rosc | Freq. | Rosc | Freq. | Rosc | Freq. | Rosc | Freq. | Rosc | Freq. |
|-------|--------|-------|--------|-------|--------|------|--------|------|--------|
| 10K | 250KHz | 30.9K | 340KHz | 61.9K | 430KHz | 105K | 520KHz | 165K | 610KHz |
| 12K | 260KHz | 34K | 350KHz | 64.9K | 440KHz | 110K | 530KHz | 174K | 620KHz |
| 14K | 270KHz | 36.5K | 360KHz | 69.8K | 450KHz | 115K | 540KHz | 182K | 630KHz |
| 16.2K | 280KHz | 40.2K | 370KHz | 73.2K | 460KHz | 121K | 550KHz | 191K | 640KHz |
| 18.2K | 290KHz | 43.2K | 380KHz | 78.7K | 470KHz | 130K | 560KHz | 200K | 650KHz |
| 20.5K | 300KHz | 46.4K | 390KHz | 82.5K | 480KHz | 137K | 570KHz | | |
| 23.2K | 310KHz | 49.9K | 400KHz | 88.7K | 490KHz | 143K | 580KHz | | |
| 25.5K | 320KHz | 53.6K | 410KHz | 93.1K | 500KHz | 150K | 590KHz | | |
| 28K | 330KHz | 57.6K | 420KHz | 100K | 510KHz | 158K | 600KHz | | |

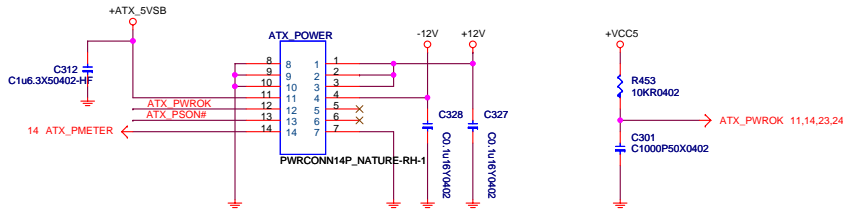
| PWM ADDRESS | |
|----------------|-----------------------------|
| RESISTOR VALUE | SVID ADDRESS FOR VCORE RAIL |
| 10K | 0000 |
| 25K | 0010 |
| 45K | 0100 |
| 70K | 0110 |
| 95K | 1000 |
| 125K | 1010 |
| 165K | 1100 |

| BOOT VOLTAGE & Phase no. | | |
|--------------------------|--------------|------------------|
| RESISTOR VALUE | BOOT VOLTAGE | Phase no. in P51 |
| 30.1K | 1.0V | 1 |
| 49.9K | 1.65V | 1 |
| 69.8K | 1.7V | 1 |
| 90K | 1.75V | 1 |
| 130K | 1.0V | 2 |
| 150K | 1.65V | 2 |
| 169K | 1.7V | 2 |
| open | 1.75V | 2 |



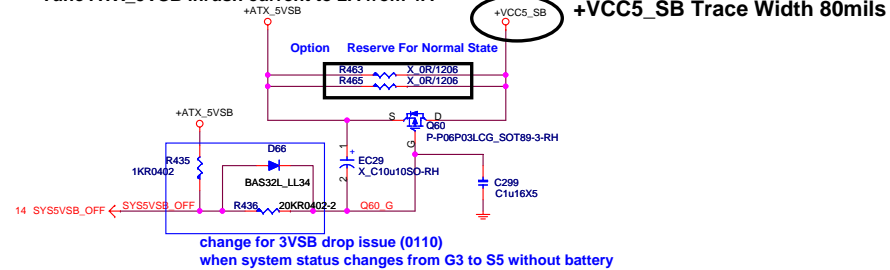
ATX Power Connector / Front Panel / LED/DSW

14 Pin ATX Power Connector

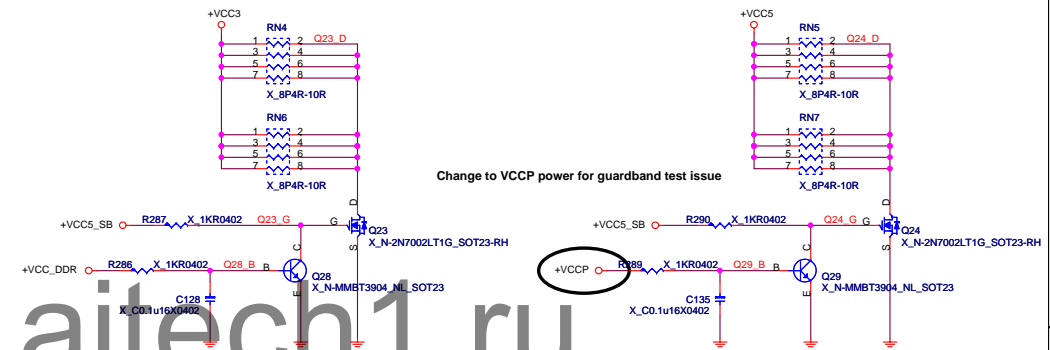


5VSB Power Switch

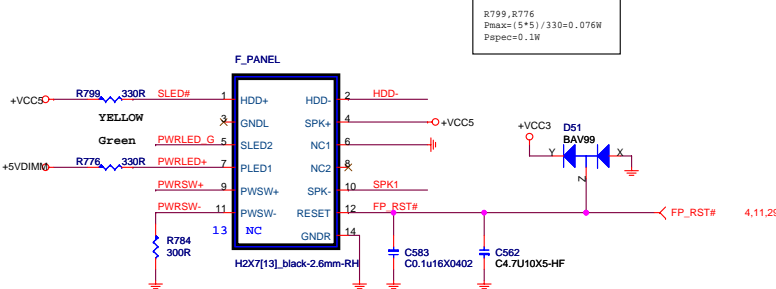
Tune ATX_5VSB inrush current to 2A from 4A



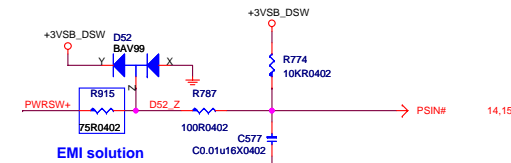
VCC3 } VCC5 Discharge Schematic



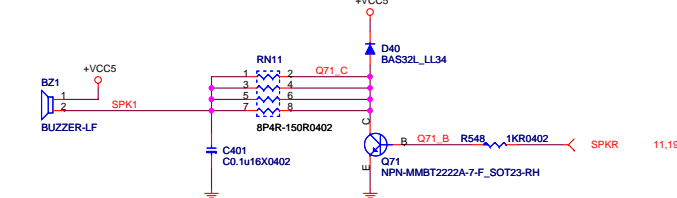
LENOVO Front Panel Connector



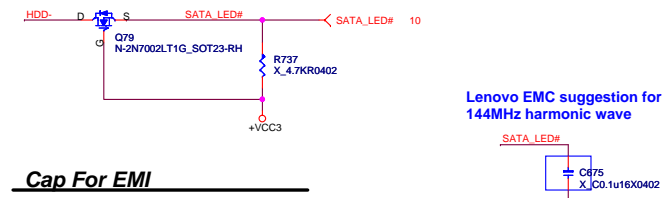
Power Button



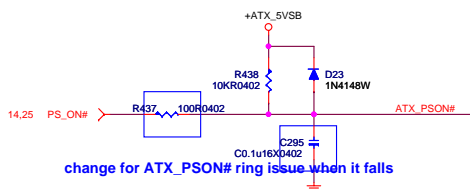
Buzzer Circuit



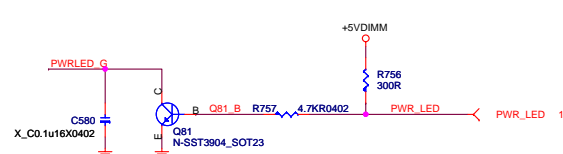
HDD LED



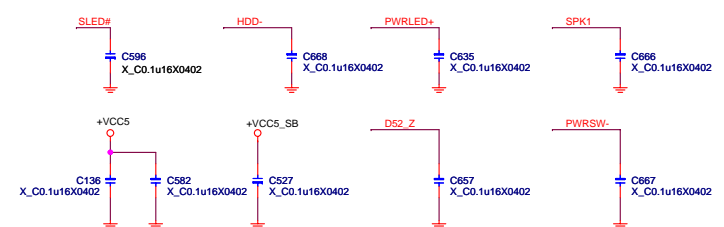
ATX Power On



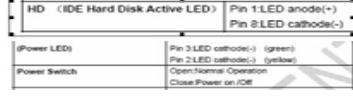
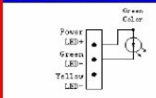
Power LED



Cap For EMI

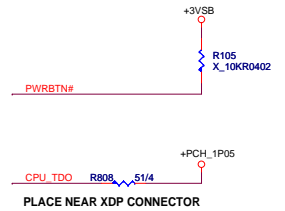
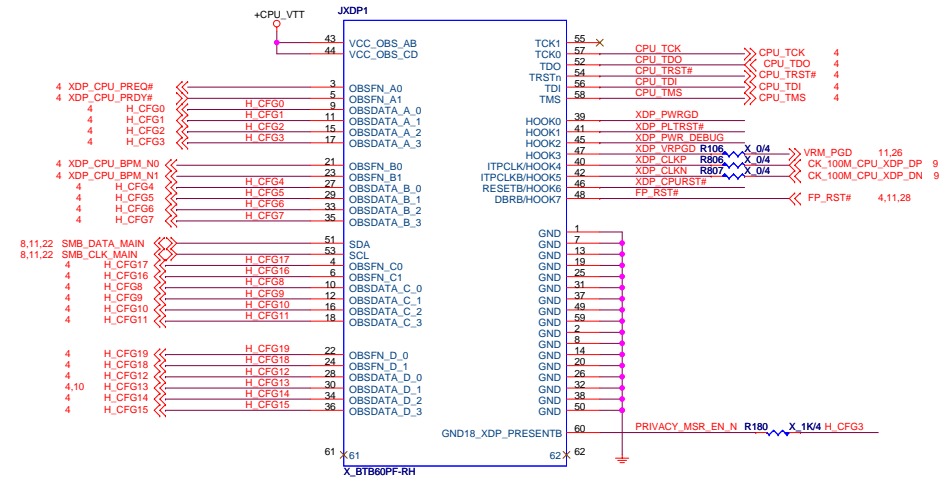


2-pin single color Power LED



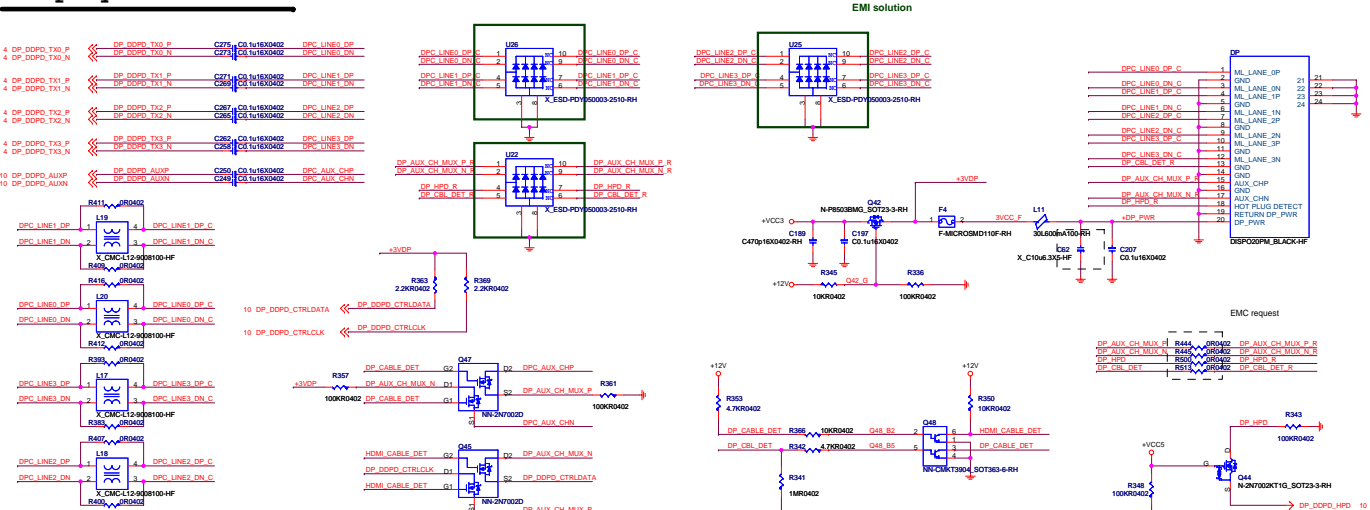
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|---------------------|----------------------------|-------|----------|
| Title | | | |
| ATX/F_Panel/EMI/LED | | | |
| Size | Document Number | Rev | |
| | IH81M | 0E | |
| Date: | Thursday, January 31, 2013 | Sheet | 28 of 36 |

Reserve debug port 5020

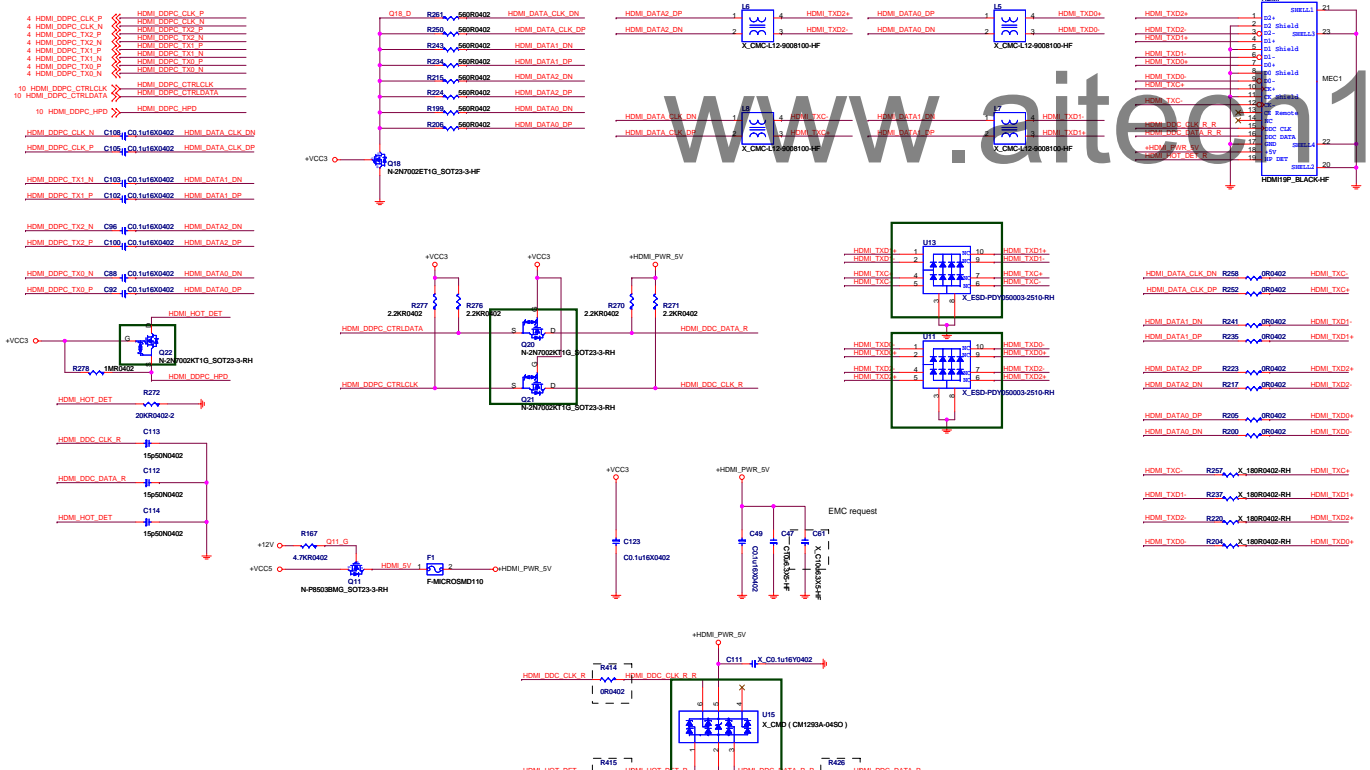


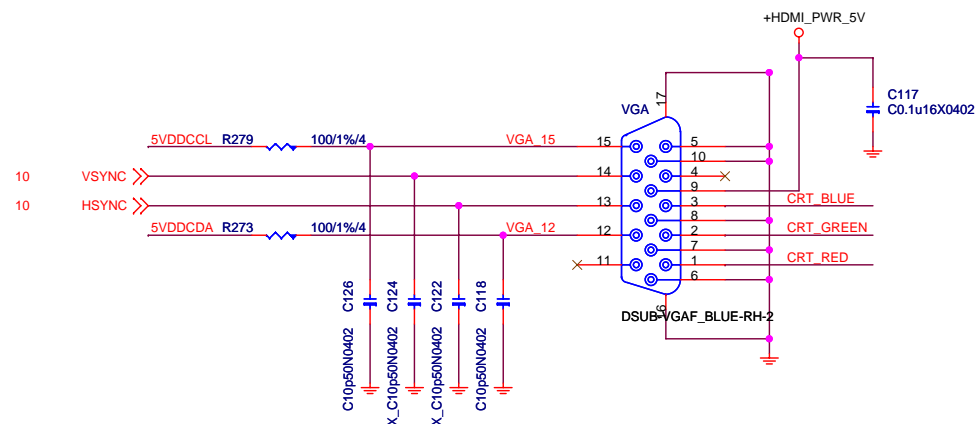
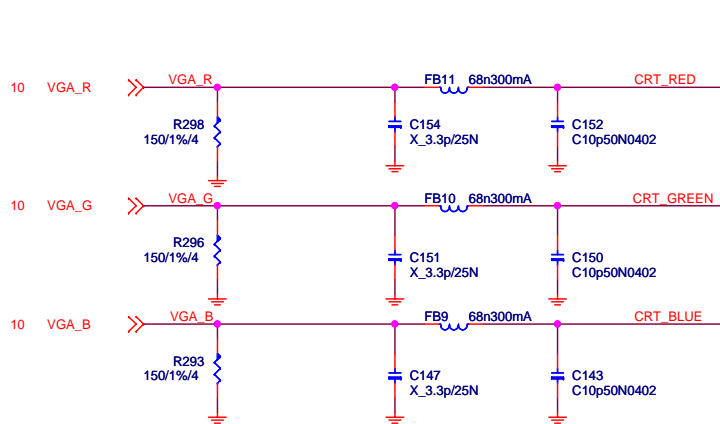
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Display Port

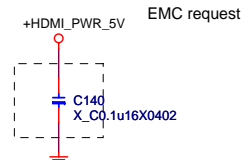
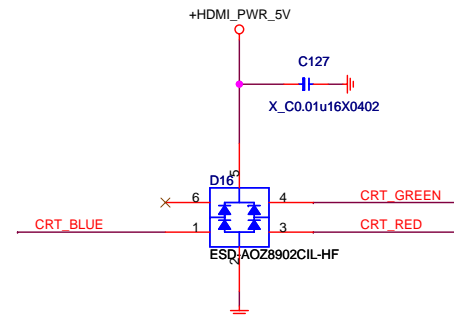
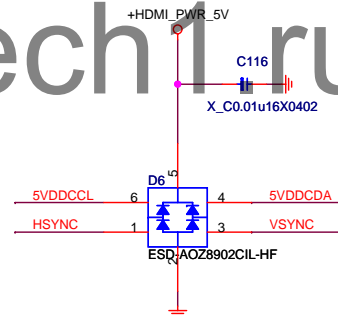
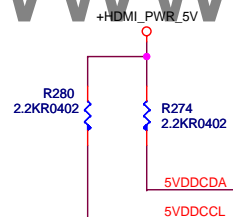
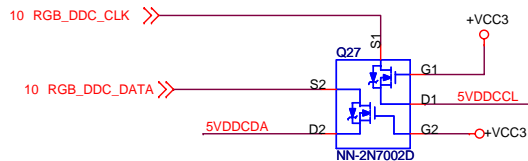


HDMI Port

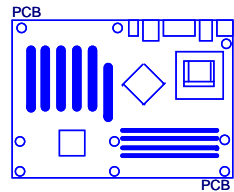




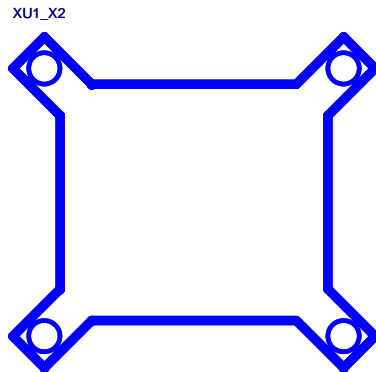
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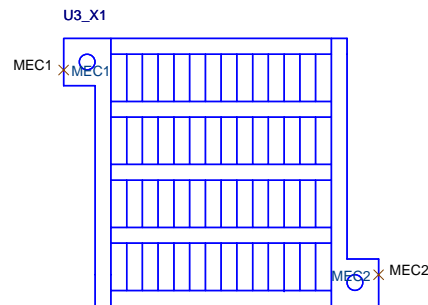
Manual Parts



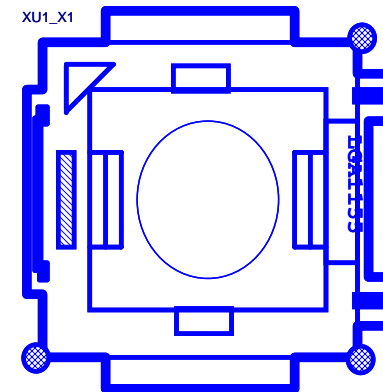
P30-0782510-E48/P30-0782510-E55



X_CPU Backplate

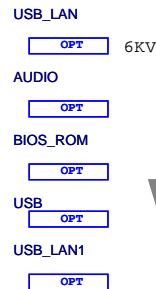
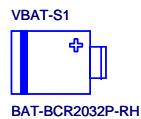
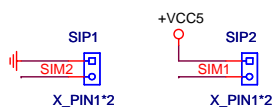


PCH Heatsink



CPU SOCKET

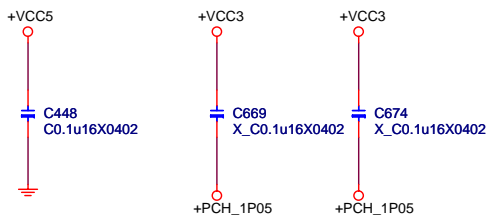
Simulation



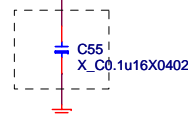
change LAN connector to N58-22F1691-F02
to use sidactor for surge protection



For EMI For Moat CAP



EMI Suggestion
VRM part has high frequency noise



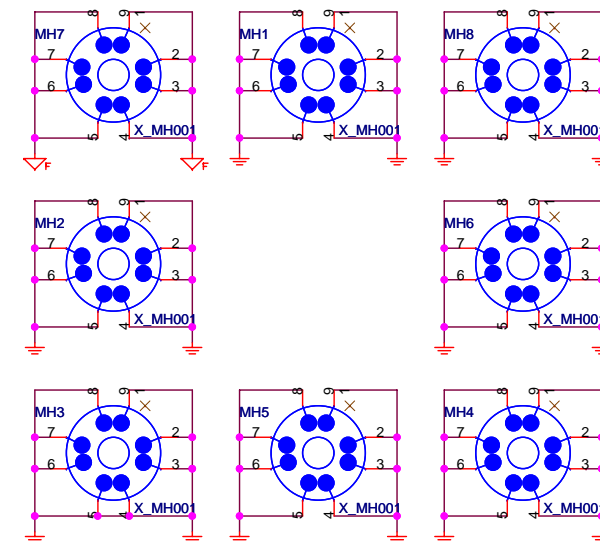
Optics Orientation Holes


Optical Fiducial Marks-120



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Mounting Holes



| | | |
|---|---------------------------------|------------------|
|  MICRO-START INT'L CO.,LTD. | | |
| Title Manual & Option Parts | | |
| Size | Document Number IH81M | Rev 0E |
| Date: | Friday, February 01, 2013 | Sheet 32 of 36 |

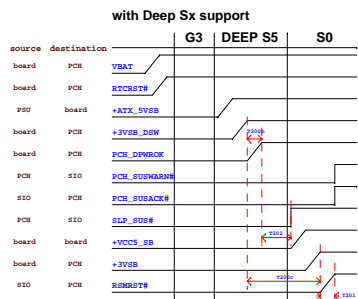
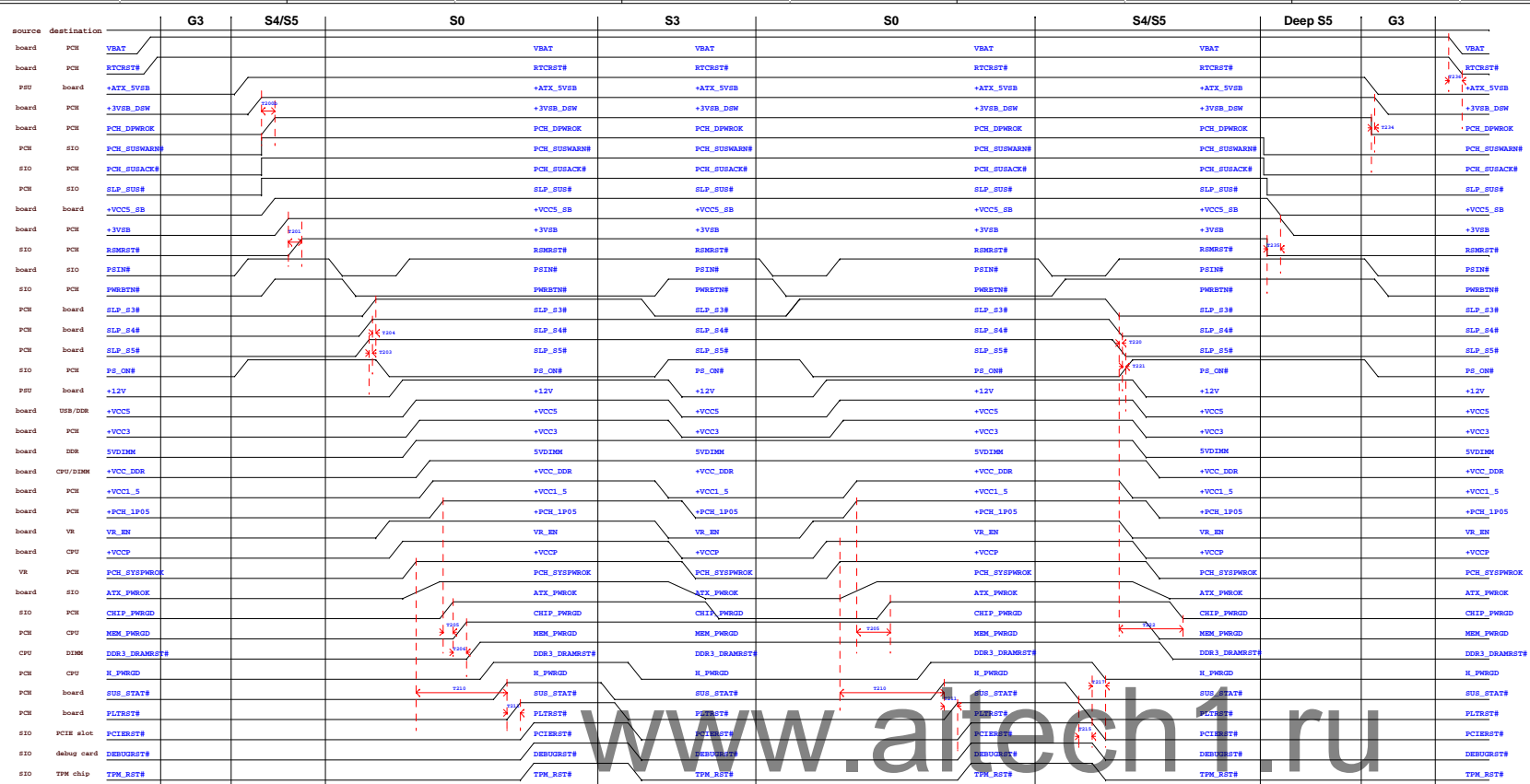


Figure 8-1. G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram

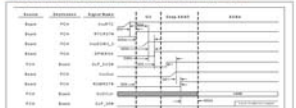
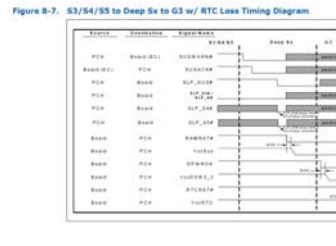
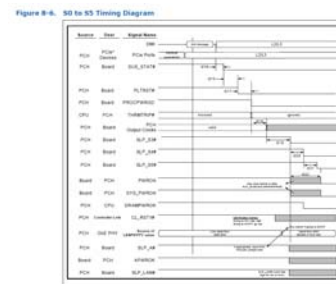
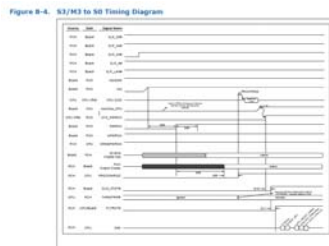
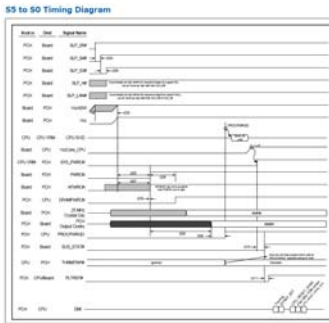
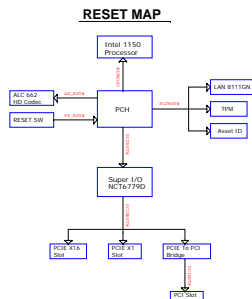
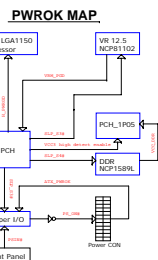


Figure 8-2. G3 w/RTC Loss to S4/S5 (Without Deep Sx Support) Timing Diagram



Note: VCC5B1 will ramp up later in comparison to VCC5B0 due to assumption that SLP_S0S# is used to control power to VCC5B1.



| PCH | | | | | | | | |
|----------|-------------------------|--------|--------|------|---------|---------------|--------------|------------------|
| GPIO | Alt Function | I/O/NC | Power | Tol | Default | Signal Name | Input/Output | Pull-Hi/Pull-Low |
| GPIO[0] | BMBSUS# | I/O | Main | 3.3V | GPI | BM_BUSY# | Input | Pull-Hi |
| GPIO[1] | Unmuxed | I/O | Main | 3.3V | GPI | PCH_GPIO1 | Input | Pull-Hi |
| GPIO[2] | PIRQE# | I/O | Main | 5V | GPI | SPL_WP#_PCH | Output | Pull-Hi |
| GPIO[3] | PIRQF# | I/O | Main | 5V | GPI | PCH_GPIO3 | Output | Pull-Hi |
| GPIO[4] | PIRQG# | I/O | Main | 5V | GPI | PCH_GPIO4 | Input | Pull-Hi |
| GPIO[5] | PIRQH# | I/O | Main | 5V | GPI | PCH_GPIO5 | Output | Pull-Hi |
| GPIO[6] | Unmuxed | I/O | Main | 3.3V | GPI | PCH_GPIO6 | Input | Pull-Hi |
| GPIO[7] | Unmuxed | I/O | Main | 3.3V | GPI | PCH_GPIO7 | Input | Pull-Hi |
| GPIO[8] | Unmuxed | I/O | Resume | 3.3V | GPO | PCH_GPIO8 | Output | Pull-Hi |
| GPIO[9] | OC5# | I/O | Resume | 3.3V | Native | USB_OC#P5 | Input | Pull-Hi |
| GPIO[10] | OC6# | I/O | Resume | 3.3V | Native | USB_OC#P6 | Input | Pull-Hi |
| GPIO[11] | SMBALERT# | I/O | Resume | 3.3V | Native | PCH_SMBALERT# | Output | Pull-Hi |
| GPIO[12] | LAN_PHY_PWR_CTRL | I/O | Resume | 3.3V | Native | LAN_DISABLE# | Output | NC |
| GPIO[13] | Unmuxed | I/O | Resume | 3.3V | GPI | PCH_GPIO13 | Output | Pull-Hi |
| GPIO[14] | OC7# | I/O | Resume | 3.3V | Native | SIO_PME# | Input | Pull-Hi |
| GPIO[15] | Unmuxed | I/O | Resume | 3.3V | GPO | PCH_GPIO15 | Output | Pull-Hi |
| GPIO[16] | SATA4GP | I/O | Main | 3.3V | GPI | PCH_GPIO16 | Input | Pull-Hi |
| GPIO[17] | Unmuxed | I/O | Main | 3.3V | GPI | CLR_CMOS | Input | Pull-Hi |
| GPIO[18] | PCIECLKRQ1# | I/O | Main | 3.3V | Native | PCH_GPIO18 | Input | Pull-Hi |
| GPIO[19] | SATA1GP | I/O | Main | 3.3V | GPI | PCH_GPIO19 | Input | Pull-Hi |
| GPIO[20] | PCIECLKRQ2# | I/O | Main | 3.3V | Native | PCIECLKREQ2# | Input | Pull-Hi |
| GPIO[21] | SATA0GP | I/O | Main | 3.3V | GPI | PCH_GPIO21 | Input | Pull-Hi |
| GPIO[22] | SCLOCK | I/O | Main | 3.3V | GPI | LPT_DET# | Input | Pull-Hi |
| GPIO[23] | LDRQ1# | I/O | Main | 3.3V | Native | LDRQ1# | Input | NC |
| GPIO[24] | Unmuxed | I/O | Resume | 3.3V | GPO | PCH_GPIO24 | Output | Pull-Low |
| GPIO[25] | Unmuxed | I/O | Resume | 3.3V | Native | PCH_GPIO25 | Output | Pull-Hi |
| GPIO[26] | Unmuxed | I/O | Resume | 3.3V | Native | PCH_GPIO26 | Input | Pull-Hi |
| GPIO[27] | Unmuxed | I/O | DSW | 3.3V | GPI | PCH_GPIO27 | Output | Pull-Hi |
| GPIO[28] | Unmuxed | I/O | Resume | 3.3V | GPO | PCH_GPIO28 | Input | Pull-Hi |
| GPIO[29] | SLP_WLAN# | I/O | Resume | 3.3V | Native | SLP_WLAN# | Output | NC |
| GPIO[30] | SUS_PWRDN_ACK/SUS_WARN# | I/O | Resume | 3.3V | GPI | PCH_SUSWARN# | Output | NC |
| GPIO[31] | Unmuxed | I/O | DSW | 3.3V | GPI | PCH_GPIO31 | Input | Pull-Hi |
| GPIO[32] | Unmuxed | I/O | Main | 3.3V | GPO | CLKRUN# | Output | NC |
| GPIO[33] | HDA_DOCK_EN# | I/O | Main | 3.3V | GPO | SPL_HOLD_GPO# | Output | Pull-Hi |
| GPIO[34] | STP_PCI | I/O | Main | 3.3V | GPI | STP_PCI# | Input | Pull-Hi |
| GPIO[35] | Unmuxed | I/O | Main | 3.3V | GPO | PCH_GPIO35 | Output | NC |
| GPIO[36] | SATA2GP | I/O | Main | 3.3V | GPI | PCH_GPIO36 | Input | NC |

| SIO(NCT679D) | | | |
|--------------|--------------|--------------|---|
| PIN NAME | USAGE | Input/Output | NOTES |
| GPIO0 | AUX-FAN1_CTL | Output | Fan speed control |
| GPIO1 | NA | NA | NA |
| GPIO2 | NA | NA | NA |
| GPIO3 | NA | NA | NA |
| GPIO4 | AUX-FAN1 | Input | Fan speed sense |
| GPIO5 | NA | NA | NA |
| GPIO6 | NA | NA | NA |
| GPIO7 | NA | NA | NA |
| GPIO10 | RIB# | Input | Com port signal |
| GPIO11 | DCDB# | Input | Com port signal |
| GPIO12 | SOUTB | Output | Com port signal |
| GPIO13 | SINB | Input | Com port signal |
| GPIO14 | DTRB# | Output | Com port signal |
| GPIO15 | RTSB# | Output | Com port signal |
| GPIO16 | DSRB# | Input | Com port signal |
| GPIO17 | CTSB# | Input | Com port signal |
| GPIO20 | KBDATA | Input | Keyboard data in |
| GPIO21 | KBCLK | Output | keyboard clock out |
| GPIO22 | MSDATA | Input | Mouse data in |
| GPIO23 | MSCLK | Output | Mouse clock out |
| GPIO24 | SIO_WAKER_R | Input | Wake up signal from LAN |
| GPIO25 | AMDPWR_EN | Input | Pin strap which disabled AMD power sequence |
| GPIO26 | NA | NA | NA |
| GPIO27 | MLED | Output | Pull high |
| GPIO30 | RESETCON# | Input | Pull high |
| GPIO31 | SDA_SIO | Output | Pull high |
| GPIO32 | SCI_SIO | Output | Pull high |
| GPIO33 | NA | NA | NA |
| GPIO34 | PRSTB# | Output | LPT signal |
| GPIO35 | PRAFD# | Output | LPT signal |
| GPIO36 | PRERR# | Input | LPT signal |
| GPIO40 | TEST_MODE_EN | Input | Pin strap which disabled test mode |
| GPIO41 | PRINT# | Output | LPT signal |
| GPIO42 | LPT_SLIN# | Output | LPT signal |
| GPIO43 | PRACK# | Input | LPT signal |
| GPIO44 | PRBUSY | Input | LPT signal |
| GPIO45 | PRPE | Input | LPT signal |

| PCH | | | | | | | | |
|----------|--------------|--------|--------|------|---------|-----------------|--------------|------------------|
| GPIO | Alt Function | I/O/NC | Power | Tol | Default | Signal Name | Input/Output | Pull-Hi/Pull-Low |
| GPIO[37] | SATA3GP | I/O | Main | 3.3V | GPI | PCH_GPIO37 | Input | Pull-Hi |
| GPIO[38] | SLOAD | I/O | Main | 3.3V | GPI | CHASSIS_ID1 | Input | Pull-Hi |
| GPIO[39] | SDATAOUT0 | I/O | Main | 3.3V | GPI | CHASSIS_ID2 | Input | Pull-Hi |
| GPIO[40] | OC1# | I/O | Resume | 3.3V | Native | USB_OC#P1 | Input | Pull-Hi |
| GPIO[41] | OC2# | I/O | Resume | 3.3V | Native | USB_OC#P2 | Input | Pull-Hi |
| GPIO[42] | OC3# | I/O | Resume | 3.3V | Native | USB_OC#P3 | Input | Pull-Hi |
| GPIO[43] | OC4# | I/O | Resume | 3.3V | Native | USB_OC#P4 | Input | Pull-Hi |
| GPIO[44] | PCIECLKRQ5# | I/O | Resume | 3.3V | Native | PCIECLKREQ5# | Input | Pull-Hi |
| GPIO[45] | PCIECLKRQ6# | I/O | Resume | 3.3V | Native | PCH_GPIO45 | Input | Pull-Hi |
| GPIO[46] | PCIECLKRQ7# | I/O | Resume | 3.3V | Native | PCH_GPIO46 | Input | Pull-Hi |
| GPIO[48] | SDATAOUT1 | I/O | Main | 3.3V | GPI | COM_GPIO1 | Input | Pull-Hi |
| GPIO[49] | SATA5GP | I/O | Main | 3.3V | GPI | PCH_GPIO49 | Input | Pull-Hi |
| GPIO[50] | Unmuxed | I/O | Main | 3.3V | GPI | FUSB_G1 | Input | Pull-Hi |
| GPIO[51] | Unmuxed | I/O | Main | 3.3V | GPO | PCH_GPIO51 | Input | NC |
| GPIO[52] | Unmuxed | I/O | Main | 3.3V | GPI | FUSB_G2 | Input | Pull-Hi |
| GPIO[53] | Unmuxed | I/O | Main | 3.3V | GPO | PCH_GPIO53 | Output | NC |
| GPIO[54] | Unmuxed | I/O | Main | 3.3V | GPI | PCH_GPIO54 | Input | Pull-Hi |
| GPIO[55] | Unmuxed | I/O | Main | 3.3V | GPO | PCH_GPIO55 | Output | NC |
| GPIO[57] | Unmuxed | I/O | Resume | 3.3V | GPI | PCH_GPIO57 | Output | Pull-Hi |
| GPIO[58] | SML1CLK# | I/O | Resume | 3.3V | Native | PCH_SML1CLK | Output | Pull-Hi |
| GPIO[59] | OC0# | I/O | Resume | 3.3V | Native | USB_OC#P0 | Input | Pull-Hi |
| GPIO[60] | SML0ALERT# | I/O | Resume | 3.3V | Native | PCH_SML0ALERT# | Output | Pull-Hi |
| GPIO[61] | SUS_STAT# | I/O | Resume | 3.3V | Native | SUS_STAT# | Output | NC |
| GPIO[62] | SUSCLK | I/O | Resume | 3.3V | Native | SUS_CLK | Output | NC |
| GPIO[63] | SLP_S5# | I/O | Resume | 3.3V | Native | SLP_S5# | Output | NC |
| GPIO[64] | CLKOUTFLEX0 | I/O | CORE | 3.3V | Native | NC | Output | NC |
| GPIO[65] | CLKOUTFLEX1 | I/O | CORE | 3.3V | Native | NC | Output | NC |
| GPIO[66] | CLKOUTFLEX2 | I/O | CORE | 3.3V | Native | NC | Output | NC |
| GPIO[67] | CLKOUTFLEX3 | I/O | CORE | 3.3V | Native | CLKOUTFLEX3_48M | Output | NC |
| GPIO[68] | Unmuxed | I/O | CORE | 3.3V | GPI | PCH_GPIO68 | Input | Pull-Hi |
| GPIO[69] | Unmuxed | I/O | CORE | 3.3V | GPI | PCH_GPIO69 | Input | Pull-Low |
| GPIO[70] | Unmuxed | I/O | CORE | 3.3V | GPI | PCH_GPIO70 | Output | Pull-Low |
| GPIO[71] | Unmuxed | I/O | CORE | 3.3V | GPI | PCH_GPIO71 | Output | Pull-Hi |
| GPIO[72] | Unmuxed | I/O | DSW | 3.3V | Native | PCH_GPIO72 | Output | Pull-Hi |
| GPIO[73] | PCIECLKRQ0# | I/O | Resume | 3.3V | Native | PCH_GPIO73 | Input | Pull-Hi |
| GPIO[74] | SML1ALERT# | I/O | Resume | 3.3V | Native | PCH_SML1ALERT# | Output | Pull-Hi |
| GPIO[75] | SML1DATA | I/O | Resume | 3.3V | Native | PCH_SML1DATA | Output | Pull-Hi |

| SIO(NCT679D) | | | |
|--------------|---------------|--------------|---|
| PIN NAME | USAGE | Input/Output | NOTES |
| GPIO46 | PRSLCT | Input | LPT signal |
| GPIO47 | RESETCON# | Output | Pull high |
| GPIO50 | SUSWARN# | Input | DSW signal |
| GPIO51 | SIO_5VDUAL | Input | DSW signal |
| GPIO52 | SUSACK# | Output | DSW signal |
| GPIO53 | NA | NA | NA |
| GPIO54 | SLP_SUS# | Input | DSW signal |
| GPIO55 | SYSSVSB_OFF_R | Output | DSW signal |
| GPIO56 | NA | NA | NA |
| GPIO57 | PWR_LED_R | Output | LED drive signal which shows the system state |
| GPIO60 | RND0 | I/O | LPT signal |
| GPIO61 | RND1 | I/O | LPT signal |
| GPIO62 | RND2 | I/O | LPT signal |
| GPIO63 | RND3 | I/O | LPT signal |
| GPIO64 | RND4 | I/O | LPT signal |
| GPIO65 | RND5 | I/O | LPT signal |
| GPIO66 | RND6 | I/O | LPT signal |
| GPIO67 | RND7 | I/O | LPT signal |
| GPIO70 | DSW_EN | Input | Pin strap which enable DSW |
| GPIO71 | NA | NA | NA |
| GPIO72 | NA | NA | NA |
| GPIO73 | NA | NA | NA |
| GPIO74 | RSTOUT0# | Output | PCIE reset signal |
| GPIO75 | RSTOUT1# | Output | LPC_Debug card reset signal |
| GPIO76 | RSTOUT2# | Output | TPM reset signal |
| GPIO80 | CTSA# | Input | COM port signal |
| GPIO81 | DSRA# | Input | COM port signal |
| GPIO82 | RTSA# | Output | COM port signal |
| GPIO83 | DTRA# | Output | COM port signal |
| GPIO84 | SINA | Input | COM port signal |
| GPIO85 | SOUTA | Output | COM port signal |
| GPIO86 | DCDA# | Input | COM port signal |
| GPIO87 | RIA# | Input | COM port signal |

| DDR-III DIMM Config | | | |
|---------------------|------------------|------------------|------------------|
| DEVICE | ADDRESS(SA1:SA0) | CLOCK | |
| DIMM 1 | 00 | MEM_MA_CLK_H0/L0 | MEM_MA_CLK_H1/L1 |
| DIMM 2 | 10 | MEM_MB_CLK_H0/L0 | MEM_MB_CLK_H1/L1 |



History

0C-0D change list

- 1. change HDD fan from 3pin no control to 4pin smart fan
- 2. reserve 0402 footprint location next to audio ESD component at all audio line of connector and pin header
- 3. add audio depop schematic for all channel of audio connector and only line out channel of front audio
- 4. connect GPIO57 to PCIE1x pin B12 to control WLAN and GPIO15 to PCIE1x pin A7 to control bluetooth for PCIE1x when wifi card plugged in PCIE1x connector
- 5. SPI_CS0_R# pull high to +VCC3, pull up resistor is 2.2k ohm. Doing this is to give Q83 S an fix voltage level and not let it floating
- 6. remove ALC662VC co-lay schematic
- 7. change LAN connector surge protection from gastube to Sidactor


0D-0E change list

- 1. remove R96 and stuff R178 due to leakage voltage on vcc3
- 2. change R11 to 29.4K, C16 to 470pf, R15 to 21K, C14 to 470pf, R30 to 137K and R79 to 34K for VRM 12.5 transient test solution
- 3. add board ID for NEC H81 bom
- 4. change R486 to 31.6K due to LAN power value is a little high when SA test power ripple noise item
- 5. add 1Kohm resistor to GND on +3VSB_DSW output due to +3VSB_DSW voltage will over spec when system changes from S0 to S5
- 6. change R702 to 33R and C508 to 15pf due to the voltage of CK_PCH_33M_FB is too big
- 7. change R893 to 33R due to the voltage of PCI_CLK0 is too big
- 8. change R690 to 33R due to the voltage of LPC_PCLK is too big
- 9. change low gate damping resistor to 0ohm in every phase due to dead time fail when test VRM power
- 10. change C524 to 180pf due to the voltage of AZ_RST# is a little big
- 11. change R436 to 200K due to 3VSB has a drop when system changes from G3 to S5
- 12. remove external pull up resistor and change C101 to 680pf due to KBRST# will have low pulse when it rises up
- 13. add LEO_CHIP 33M clock
- 14. change C476/C477 to 15pf for more precise 32.678KHz frequency
- 15. EMI solution: change R816/R817/R819/R820 to 300R bead
- 16. EMI solution: add 75R resistor on PWRSW+ trace
- 17. change C295 to 0.1uf and R437 to 100R for ATX_PSON# ring issue when it falls
- 18. mounted VCC5 enable schematic and delay VCC3 enable after VCC5 enable for VR_PG step issue
- 19. mounted L13/L14 for Lenovo EMC request
- 20. add one cap on SATA_LED# for EMC 144MHz harmonic wave issue
- 21. change C254 to 6.8nf, R376 to 14.7K, R370 to 16.2K, EC25 to unstuff to set VCC5 OCP to 35A
- 22. change C43 to 1uf to reduce VCC5 inrush current
- 22. change PCIE standby power to 3VSB as it don't need power at deep S5
- 23. add R875 for PCI wake debug
- 24. add R916 for Lenovo DCL1.8 DDR module new request
- 25. change LAN power source to 3VSB as LAN don't need power in deep s5
- 26. remove 3VA_PCIE schematic as it don't need any more
- 27. change R11 to 30K for lout function and keep R79 value the same with 0C
- 28. add LAN wake switch in page14
- 29. change ME auto recovery schematic for logic error
- 30. change U15/U11/U13/U22/U25/U26 to unstuff; change Q20/Q21/Q22/Q44 PN to D03-7002K69-005
stuff D13/D14 and stuff L10/L12/L15/L16
- 31 U28/U29 can be unmounted if LAN connector has surge protect
- 32 add without LAN surge connector for Malmo and Toulouse
- 33 change DDR external CA/DQ voltage reference component to stuff as internal ref is very unstable
- 34 change R11 to 30.9K/R99 to 75K/R15 to 22.6K to meet intel new lmax 95A

0E-1.0 change list

- 1. add ME auto recovery schematic
- 2. change R134 to 10.7K for power solution
- 3. change R789/R801 to 33R for audio precision test fail
- 4. reserve 1.05V control VR EN schematic
- 5. modify T205/T206 sequence in Reset/Pwrok/PON page
- 6. change fan name to capital
- 7. reserve LAN wake switch schematic as it can wake up the system when system state changes from G3 to S5 with 09A BIOS
- 8. add 1000pf cap on chip_pwrgrd on SIO side for SA test
- 9. add RC delay circuit for DDR switching power. VCC of the chip should be valid earlier than EN
- 10. modify 5VSB contorl schematic as it will have issue from G3 to S5 in without battery condition
- 11.change R102/R103/R117/R118/R127/R128/R139/R140 to 10K to reduce draw current
- 12. change R722/R721 to 10Kohm
- 13. change EC11 to unstuff, EC10 to stuff for maunfactory
- 14. change XDP part to reserve, stuff R808

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